1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	26 April 1993	Annual Technical(1 Aug 92-31 Jan 93)

4. TITLE AND SUBTITLE
Optically Powered, Optoelectronic Spatial Light Modulators

5. FUNDING NUMBERS
F49620-92-J-0432

6. AUTHOR(S)
Stephen R. Forrest

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Princeton University
ATC/POEM
Dept. of Electrical Engineering
Princeton, NJ 08544

8. PERFORMING ORGANIZATION REPORT NUMBER
AFOSR-TR- 93 0351

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
AFOSR/PKA
110 Duncan Avenue
Suite B115
Bolling AFB, DC 20332-0001

NE

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
2301 DS

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT
unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

We describe a program which endeavors to make significant progress towards the realization of very high density, fast, InP-based optoelectronic spatial light modulators (SLMs). The central concept of the devices is to eliminate as many contacts to the SLM as possible by supplying integral, "local" circuit power and control via the connection of the active circuit to integrated photovoltaic (PV) cells. Power to the circuits is thereby supplied by a bright light source operating at a different wavelength than the optical data channel. The SLM will be fabricated in InP-based materials due to the ease of integration of photovoltaic cells (used in providing circuit power and control), with high bandwidth transceiver optoelectronic integrated circuits (OEICs). Work includes materials and device fabrication, packaging and systems demonstrations.

In addition to applications in optical interconnection and optical computing, such "contactless" circuit concepts can also be applied to many diverse systems such as for providing highly synchronous optical clock signals on VLSI chips, and for powering OEICs placed at the end of remote probes where size, power, and environmental restrictions prohibit the placement of the power source adjacent to the active electronics. We are engaged in a broad program directed at investigating the fundamental limits confronting materials, devices, circuits and systems which make use of the family of novel devices which are based on the optical powering concept.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Smart Pixels, Optoelectronic Integrated Circuits, Spatial Light Modulators	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
unclass	unclass	unclass	UL

Contract No: F49620-92-J-0432

Title: Optically Powered, Optoelectronic Spatial Light Modulators

Principal Investigor: Stephen R. Forrest

Advanced Technology Center for Photonics and Optoelectronic Materials
Department of Electrical Engineering
Princeton University
Princeton, NJ 08544

Reporting Period: August 1, 1992 to January 31, 1993

Prepared for: Dr. Alan Craig

AFOSR/PKA
110 Duncan Avenue
Suite B115
Bolling AFB, DC 20332-0001

Optically Powered, Optoelectronic Spatial Light Modulators

Stephen R. Forrest
Advanced Technology Center for Photonics and Optoelectronic Materials
Department of Electrical Engineering
Princeton University
Princeton, NJ 08544

Period of Performance: 8/1/92 to 2/28/93

The work during this first period of the grant to investigate the limits of high bandwidth, high gain smart pixels has focussed on two areas: Analysis of the limits of smart pixel technologies, and the design of a prototypical, high performance integrated smart pixel. The pixel being pursued is a high bandwidth spatial light modulator (SLM) pixel with gain and low power dissipation. We now discuss in detail some of the results achieved in the first six months of the program.

I. Analytical comparison of various smart pixel technologies. Here, smart pixel NOR gates were used as a basis to compare, from first principles, the fundamental processes which determine the performance of 2D smart pixel arrays employing either optoelectronic (i.e. detector/logic circuit/laser) or SEED based technologies. In this analysis, such factors as device noise and input power sensitivity, bandwidth, power dissipation, switching energy, temperature and wavelength sensitivity were all considered from a system/device performance perspective. It was found that a useful "figure of merit" for 2D smart pixel arrays is the information flux density, $F = B\rho$. Here, B is the bandwidth per channel in the array, and ρ is the number of pixels per unit area which is typically constrained by power dissipation. Assuming a maximum power dissipation of 1 W/cm^2 for the array, the optoelectronic (and in some cases FET-SEED arrays) can have $F = 200$ GHz/cm^2 at a maximum channel bandwidth approaching 10 GHz. This is compared with SEED-based arrays, which typically have a limitation of 1 - 10 GHz/cm^2 at a channel bandwidth of 10 - 100 MHz. This study goes further, to compare optoelectronic smart pixel technologies to Si CMOS.

A second result is that, for the first time, we analyzed the basic switching noise processes in SEED devices. Understanding switching noise is central to

determining the range of applicability of any particular technology to a given system application, and hence it is important that such calculations be done to ascertain the potential performance of SEED-based switches in networks. Our conclusion is that SEEDs are shot noise limited, and can achieve low bit error rate operation only under certain well defined ranges of bandwidth and input power (which must be traded off against each other). We regard this "first principles" calculation as an essential step in the utilization of any bistable switching technology in a particular system environment.

Both of these studies have been detailed in the manuscripts provided in Appendix I. These are:

1. "Implementations of Smart Pixels for Optoelectronic Processors and Interconnection Systems. I. Optoelectronic Gate Technology", S. Yu and S. R. Forrest, *IEEE J. Lightwave Technol.*, accepted (1993).

2. "Implementations of Smart Pixels for Optoelectronic Processors and Interconnection Systems. II. SEED-Based Technoloogy and Comparison with Optoelectronic Gates", S. Yu and S. R. Forrest, *IEEE J. Lightwave Technol.*, accepted (1993).

3. "Switching Noise in Self-Electrooptic Effect Device Logic Gates", S. Yu and S. R. Forrest, *Appl. Phys. Lett.*, submitted (1993).

II. Spatial Light Modulator Design. In a second line of investigation, we have begun the process of demonstrating a smart pixel circuit which tests the limit of performance of optoelectronic pixel technology. For this purpose, our research has focussed on the design of a very high bandwidth, low power dissipation spatial light modulator array. The circuit for this device is shown in Fig. 1.

This circuit, which will be fully integrated using the InGaAs/InP materials system, has the ability to be either optically or electrically controlled. The optical input data signal is incident on the p-i-n detector which is approximately 40 μm in diameter. This signal is then amplified using a negative-feedback, stable front-end HBT amplifier which then drives one of a differential pair of transistors in the output, or "transmitter" stage. The second transistor of the output pair serves as the current source for the output laser. Optical control is effected by illuminating a photoconductor with a short wavelength (0.82 μm) control beam, P_C. This photoconductor is in series with the emitter resistor of the front end FET, and hence it "enables" the receiver front-end circuit. We will fabricate the

photoconductor using an interdigitated pattern of electrodes placed directly onto the surface of the semi-insulating InP substrate. In those circuits where only electrical control is desired, the photoconductor will be replaced by a patterned interconnect between the emitter resistor and ground.

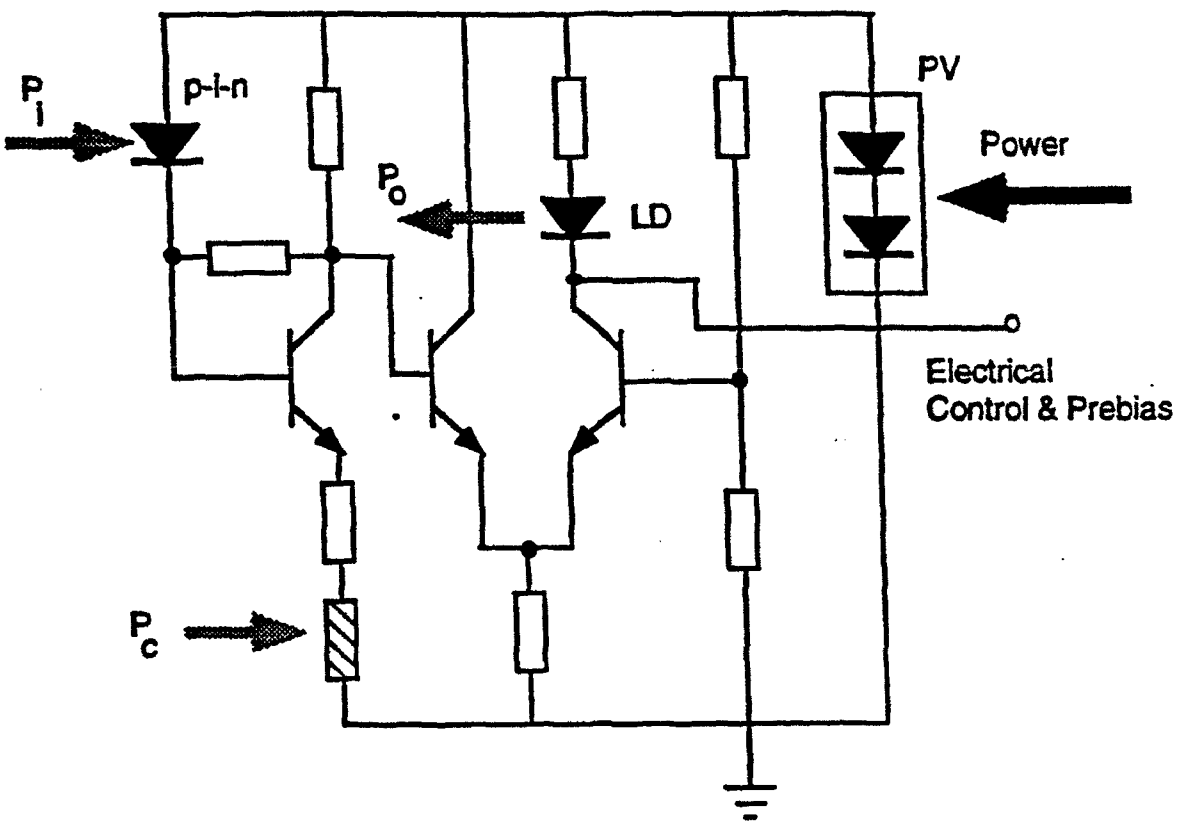


Figure 1: SLM Circuit

Electrical enable, or control of the SLM, as well as laser pre-bias, is provided by an electrical contact placed at the cathode of the laser diode. Presently, we are considering two different approaches to laser integration. The initial circuits will have longitudinal lasers bonded onto accepting pads in the circuits. These lasers will be mounted adjacent to 45° mirrors which will reflect the light normal to the wafer surface. In the second generation SLM array, integrated lasers with RIE etched angled mirrors will be employed.

Finally note that the circuit above employs photovoltaic (PV) powering. This type of powering, which has been shown in previous work to greatly reduce

cross-talk between pixels, will be integrated in some (but not all) pixel arrays to test their utility in this particular application.

We have SPICE modelled the circuit in Figure 1 and have found the following performance characteristics assuming a laser threshold current of 1 mA:

- Pixel power dissipation = 7.5 mW
- Supply Voltage: 3V
- Bandwidth: 1.4 GHz
- Optoelectronic gain: 10 dB

The frequency response of the pixel is shown in Fig. 2. Note that the threshold current assumed for this pixel is quite small. Thus, a prebias line is placed in the circuit in Fig. 1. If we assume a pixel power dissipation of 10 mW is acceptable (leading to a packing density of 100 cm^{-2} for a total power dissipation of 1 W/cm^2 in a passively cooled chip), this implies that the allowable threshold current can be approximately 3.5 mA. This value is certainly easier to obtain than 1 mA, although it still implies that very high quality lasers must be employed. However, if we use active cooling (i.e. if a TE cooler is employed), then even higher laser thresholds can be tolerated.

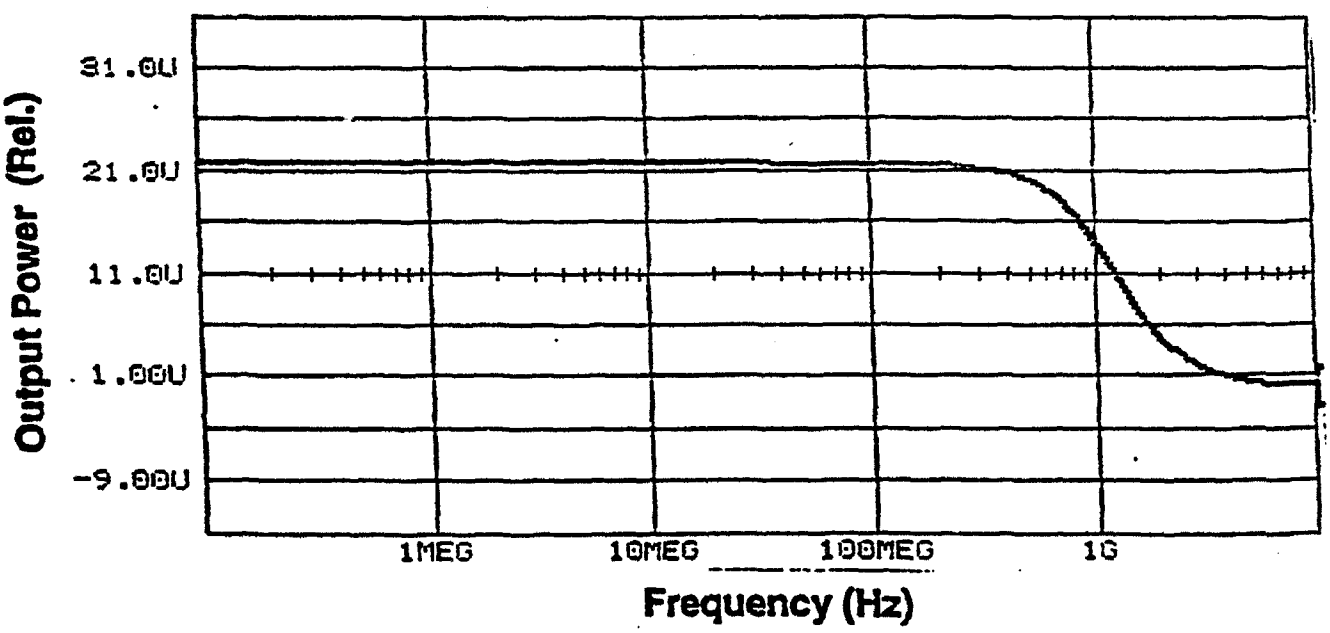


Figure 2: Frequency response of the SLM in Fig. 1.

Nevertheless, these performance parameters are excellent, and should make this SLM smart pixel technology highly competitive with alternative means. In addition, the low supply voltage makes PV powering extremely attractive. We have already begun to design the wafer structure and layout for the pixel, and this work will continue to be pursued in the coming months such that an integrated SLM can be demonstrated in the near future.

III. Personnel supported under AFOSR sponsorship

- Song Yu: Princeton University, PhD student.

Appendix I

Papers submitted to Journals Reporting work supported by this AFOSR grant

1. "Implementations of Smart Pixels for Optoelectronic Processors and Interconnection Systems. I. Optoelectronic Gate Technology", S. Yu and S. R. Forrest, *IEEE J. Lightwave Technol.*, accepted (1993).

2. "Implementations of Smart Pixels for Optoelectronic Processors and Interconnection Systems. II. SEED-Based Technoloogy and Comparison with Optoelectronic Gates", S. Yu and S. R. Forrest, *IEEE J. Lightwave Technol.*, accepted (1993).

3. "Switching Noise in Self-Electrooptic Effect Device Logic Gates", S. Yu and S. R. Forrest, *Appl. Phys. Lett.*, submitted (1993).

Revised

Implementations of Smart Pixels for Optoelectronic Processors and Interconnection Systems I. Optoelectronic Gate Technology

Song Yu and Stephen R. Forrest
Advanced Technology Center for
Photonics and Optoelectronics Materials (ATC/POEM)
Department of Electrical Engineering
Princeton University
Princeton, NJ 08544

Abstract

Smart pixels are an emerging technology for implementing optical interconnections and optoelectronic computing systems. We have studied several of the common approaches to smart pixel technology, including smart pixels based on optoelectronic integrated circuits and self-electro-optic effect devices (SEEDs). In this first of two papers (Paper I), an optoelectronic NOR gate pixel consisting of an output laser diode, two input photodetectors, and a transistor circuit is analyzed for the purpose of investigating overall two dimensional (2D) interconnection and processing system performance. We then analyze and discuss the major pixel performance issues. The results show that the optoelectronic logic gate has the advantages of low noise (typically $\sim -35dBm$), high bandwidth ($> 1GHz$) and low temperature sensitivity while its power dissipation is about $5mW$, resulting in a moderate pixel packing density of $200/cm^2$ for a total chip power dissipation of $1W/cm^2$. In the subsequent paper (Paper II), we analyze a similar, SEED-based logic element and compare its performance to the optoelectronic approach studied here.

Table of Symbols for Paper I and Paper II

A	device area
B	bit rate
B_{co}	cutoff bit rate of SEED based logic gates
β	transistor current gain
C_b	base-charging capacitance of the transistor
C_d	photodiode capacitance
C_{je}	base-emitter capacitance of the transistor
C_M	Miller capacitance
C_μ	base-collector capacitance of the transistor
C_π	$C_b + C_{je}$
C_s	stray capacitance
C_t	total input capacitance of the photoreceiver
C_{tot}	total capacitance of the S-SEED
CR	contrast ratio
D	decision level
d	device thickness
δ	mass density
$\mathcal{E}$	electric field
$\mathcal{E}_g$	bandgap
E_{sw}	switching energy
η_c	optical coupling efficiency
η_d	external quantum efficiency of laser diode
η_{sp}	spontaneous emission efficiency of laser diode
η_{ph}	quantum efficiency of photodiode
F	fanout
$\mathcal{F}$	information flux
Δf	bandwidth (3dB)
G	optoelectronic gain of a single stage interconnect
g_m	transistor transconductance
$h\nu$	photon energy
I_0	current constant of laser threshold
I_2	Personick integral
I_3	Personick integral
I_b	base current of HBT
I_c	collector current of HBT
I_g	gate leakage current of FET
I_{th}	threshold current of laser diode
I_{ld}^{on}	laser current of the on state

I_{ld}^{off}	laser current of the off state
ΔI_{th}	change of threshold current of laser diode
$< i^2 >$	noise current
$< i_q^2 >$	quantum noise current of SEED
$< i_{FS}^2 >$	noise current of FET-SEED
λ	wavelength
κ	thermal conductivity
m	mass
N_0	average number of photons absorbed by SEED
$\bar{P}$	photoreceiver sensitivity
$p(E)$	probability of having a switching error
P_{clk}	power of reading (or clock) beam of SEED
P_{min}	minimum input power required for a given SEED BER
P_d	average power dissipation
P_{in}	input power of S-SEED
$P_{in}(on)$	input power of the on state
$P_{in}(off)$	input power of the off state
$P_{out}(on)$	output power of the on state
$P_{out}(off)$	output power of the off state
ρ	pixel packing density
Q	signal to noise ratio for a given BER
q	electron charge
R	bias resistance in FET-SEED
R_B	bias resistance in optoelectronic NOR gate
R_L	load resistance in optoelectronic NOR gate
R_T	thermal resistance
R_{ld}	laser diode resistance
R'_L	$R_L \| R_{ld}$
r_b	base resistance of the transistor
r_π	dynamic resistance of the transistor
$S(V)$	responsivity of SEED as a function of bias voltage
s_i	digital signal level
σ_i	standard deviation of s_i
T	temperature
T_0	characteristic temperature of laser threshold
$T(0)$	transmission coefficient of SEED at "off"
$T(V_0)$	transmission coefficient of SEED at "on"
τ_F	base transit time
τ_T	thermal time constant
Δt	bit time slot
V_0	power supply of S-SEED
V_2	voltage at the node between the two SEEDs in a S-SEED
V_{cc}	power supply for optoelectronic NOR gate

Implementations of Smart Pixels for Optoelectronic Processors and Interconnection Systems I. Optoelectronic Gate Technology

Song Yu and Stephen R. Forrest
Advanced Technology Center for
Photonics and Optoelectronics Materials (ATC/POEM)
Department of Electrical Engineering
Princeton University
Princeton, NJ 08544

1 Introduction

The difficulty of implementing high density interconnections at high frequency with conventional integrated electronic circuits has led to the search for alternatives that use photons as the carrier of information [1-3]. As a result, much effort has been made to develop photonic switching technology. One particularly promising approach is based on smart pixels, which can be defined as autonomous circuits or devices that can perform a logic, amplification, switching, or other nonlinear function on incident light signals. An ideal smart pixel should be able to offer the strengths of optics in communications such as high bandwidth and parallelism, and yet preserve the advantages of electronics in information processing, such as a high degree of functionality.

The essential process in photonic switching is the modulation of light signals, which can be accomplished either by direct source modulation or external modulation. In a source

modulation system as shown in Fig. 1(a), light is detected and then converted to an electrical signal. The information embodied in the electrical signal is then processed by conventional electronic integrated circuits, and subsequently reconverted to an optical signal by using an output laser diode. Through this optical-electrical-optical cycle, it is the current in the laser diode that is modulated. This approach is represented by laser-photodetector-based optoelectronic smart pixel circuits[4-6]. In the external modulation system as shown in Fig. 1(b), the intensity of a light signal is modulated when it passes through the medium of a modulator. One of the most frequently investigated modulator structures is the self-electro-optic effect device (SEED)[7, 8]. Although smart pixels based either on optoelectronic integrated circuits (OEICs) or SEEDs have been been demonstrated, little work has been done in comparing the fundamental advantages and limitations of these two different approaches. Nevertheless such a comparative study should be helpful in our understanding of their ultimate usefulness in the context of optical interconnection and optical processing system performance.

The virtue of smart pixels is their capability of performing various logic functions on a light signal. For example, a NOR gate configured using either OEIC or SEED technology can serve as the basis for such a comparison since all Boolean logic operations can ultimately be performed using combinations of such gates. Therefore it is illustrative to compare the performance of two NOR gates; one based on OEIC, and the other on SEED technology. In this paper, we will first (Section 2) configure an optoelectronic NOR gate as the basis of our study. We will then analyze the performance of the gate in terms of noise (Section 3), bandwidth (Section 4), power dissipation (Section 5), temperature sensitivity (Section 6) and sensitivity to variations in laser threshold current (Section 7). Finally, in Section 8, a brief summary of the optoelectronic approach will be given. In a subsequent paper (Paper II), a similar analysis of SEED-based smart pixel technology will be presented. In

Paper II, we will also compare the two approaches from a system perspective. We note that in order to clearly compare device and system performance, we use a figure of merit known as "information flux", which is defined as the data throughput per unit area of an interconnection plane used in cascaded, parallel pixel matrices such as those currently being investigated for a broad range of optical interconnection and processing applications [9-10].

2 Optoelectronic NOR Gates

A schematic optoelectronic NOR gate is shown in Fig. 2a. It is composed of a laser diode (as the output device) and two photodetectors (as the inputs). In recent years, rapid progress has been made in demonstrating OEICs. Semiconductor laser diodes with submilliampere threshold current have been demonstrated in the $\lambda = 0.85 - 1.5\mu m$ wavelength range[11-15]. Figure 2b is the same NOR gate except that two additional common-base HBTs are used in a cascode configuration, giving this latter structure improved high frequency performance[16], although the resulting pixel is somewhat more complicated and power dissipative than that in Fig. 2a.

High bandwidth integrated photoreceivers in the same wavelength range have also been developed by using various component technologies including p-i-n photodiodes, field effect transistors (FET), heterojunction bipolar transistors (HBT), and heterojunction bipolar phototransistors (HPT)[17-20]. Since high bandwidth photoreceivers composed of bipolar transistors have lower noise than those composed of FETs, we choose bipolar transistor preamplifiers for the two gate inputs, or optical "receivers". These optical receivers can be either combinations of p-i-n photodiodes and HBTs, or can employ phototransistors as both detector and preamplifier. Since large device area is convenient for photodetection, the HPT

approach tends to be slower than the combination of a p-i-n detector and a small-area HBT due to the large base-emitter junction capacitance of the HPT. Therefore, in this paper we will analyze a p-i-n photodiode and a HBT as the components for the NOR gate input. We also assume that both the laser diodes and the photoreceivers operate at $\lambda = 1.3\mu m$ or $0.8\mu m$ wavelength, and are based on the InP or GaAs compound semiconductor systems, respectively.

When neither of the p-i-n photodiodes at the two gate inputs are illuminated, the laser diode at the output is biased above threshold so that the optical output is high, which is defined as logical "1". When either or both of the photodiodes are illuminated, current will be shunted from the laser diode so that it is biased below threshold, and the optical output level is low, giving a logical "0". Therefore the circuit functions as a NOR gate with optical inputs and output. When the output is "1", the optical output power per laser facet is given by:

$$P_{out}(on) = \frac{h\nu}{2q}[\eta_d(I_{ld}^{on} - I_{th}) + \eta_{sp}I_{th})]. \tag{1}$$

Here $h\nu$ is the photon energy, q is the charge of an electron, η_d is the differential quantum efficiency of the laser diode above threshold, η_{sp} is the efficiency of spontaneous emission (where $\eta_{sp} \ll \eta_d$), and I_{th} is the threshold current. The total current drawn from the DC power supply consists of the laser driving current, I_{ld}^{on}, and the photodiode dark currents. The dark current in a p-i-n photodiode is typically less than $10nA$ [21], while the driving current of the laser is in the milliampere range. Thus the total power consumption is given by $V_{cc}I_{ld}^{on}$, where V_{cc} is the power supply voltage. When either of the photodiodes is illuminated, the photocurrent is given by:

$$I_{ph} = \frac{q\eta_{ph}}{h\nu}P_{in}(on), \tag{2}$$

where η_{ph} is the quantum efficiency of the p-i-n photodiode, and $P_{in}(on)$ is the incident light power. A sufficiently large photocurrent will turn on the HBT and drive it into saturation, in which case the collector current of the transistor is independent of the voltage. Then the voltage from collector to emitter, i.e. the voltage drop across the laser diode, will decrease to the saturation voltage, thus turning the laser diode off. The optical output power per facet is then given by:

$$P_{out}(off) = \frac{h\nu}{2q}\eta_{sp} I_{ld}^{off}, \tag{3}$$

where the laser driving current, I_{ld}^{off}, is smaller than the laser threshold current, I_{th}.

In order for the output to be sensitive to the change at the input, R_B has to be sufficiently large to provide the required circuit gain. The value chosen for R_B determines gain, bandwidth, noise, and switching energy of the logic gate, and therefore is an important factor in gate design and performance. Normally, R_B is large enough to direct most of I_{ph} to the base of the HBT, i.e. $I_{ph} \simeq I_b = I_c/\beta$, where I_b and I_c are the base and collector currents of the HBT, respectively, and β is the small-signal current gain of the HBT. Here, the I_c needed to switch the laser is given by $I_{ld}^{on} - I_{ld}^{off}$. For simplicity, we assume that the laser diode current swings symmetrically about the threshold as it is being turned on and off, i.e.:

$$I_{ld}^{on} - I_{th} = I_{th} - I_{ld}^{off} = I_{th}/2. \tag{4}$$

Thus $I_c = I_{th}$. We will use this relationship between I_c and I_{th} throughout our analysis unless otherwise noted.

3 Noise Analysis

Noise performance is one of the defining characteristics of an optoelectronic receiver circuit[22]. In a cascaded interconnection/processing system, the output power at one stage is the input power at the following stage. There exists a minimum optical input power (P_{min}) that is necessary for the photoreceiver to maintain a certain bit error rate (BER) at a given operational bit rate. In order to compensate for coupling losses and to achieve fanout, the output power of each stage must satisfy the following condition:

$$P_{out}\eta_c/F \geq P_{min}, \tag{5}$$

where η_c is the optical coupling efficiency between stages, and F is the fanout defined as the maximum number of pixels that can be switched by the output from a single pixel in the preceding stage. Since the output power is modulated by the current of the laser diode, which in turn determines the gain-bandwidth and power dissipation of the pixel, it is important to understand the factors that limit P_{min}.

Starting with the small signal equivalent circuit for Fig. 2a shown in Fig. 3a, the total input capacitance of one branch of the NOR gate, C_t, is given by:

$$C_t = C_d + C_s + C_\pi + C_M. \tag{6}$$

Here C_d is the photodiode capacitance, C_s is the stray capacitance, C_π is the sum of the base-charging and the base-emitter junction capacitances, and C_M is the Miller capacitance given by $C_M = (1 + g_m R'_L)C_\mu$, where $g_m = qI_c/kT$ is the transconductance, $R'_L = R_L \| R_{ld}$ is the resistance of the load (R_L) in parallel with the laser diode (R_{ld}), and C_μ is the base-collector capacitance.

The photodiode capacitance, C_d, is determined by the absorption layer thickness which must be sufficient to achieve high quantum efficiency, but thin enough to have high bandwidth. For example, assuming a carrier velocity for InGaAs of $0.1\mu m/ps$, and if the transit time is $< 100ps$, then the thickness of the p-i-n absorption region should be less than $10\mu m$. On the other hand, the absorption coefficient of direct bandgap semiconductors is $\sim 10^4/cm$, which gives an absorption length of $1\mu m$. Thus, an intrinsic region thickness of $\geq 1\mu m$ is desirable to ensure efficient photodetection.

The area of the p-i-n diodes can also be reduced to decrease the capacitance, but is ultimately limited by the optical alignment technology used to interconnect stages in a two dimensional (2D) cascaded network. Here, we assume a detector area of $20 \times 20\mu m^2$ in our model to allow for a reasonably large light-sensitive area. This gives a capacitance of $40fF$ for a $1\mu m$ thick intrinsic region. The stray capacitance, $C_s \simeq 40fF$, is due to the metal connection between the p-i-n diode and the transistor [25]. For the HBT, the base-charging capacitance, C_b, is given by the product of base transit time, τ_F, and the transconductance, g_m. For a $500\mathring{A}$ thick InGaAs base of an InP/InGaAs HBT, the average velocity of electrons is about $5 \times 10^7 cm/s$ [26], which gives $\tau_F \simeq 100fs$. This makes C_b negligible compared to C_{je}, the capacitance of the forward biased base-emitter junction. Thus $C_\pi \simeq C_{je}$, which is several hundred femto-Farads for an emitter thickness of several thousand $\mathring{A}$. Finally, C_μ is determined by the base-collector junction area and collector thickness. For a $5 \times 5\mu m^2$ junction area and a thickness of $0.5\mu m$, $C_\mu \simeq 5fF$.

The mean square equivalent input noise current of a circuit such as in Fig. 2 is the sum of the shot noise of the base and collector currents, and the Johnson noise of the base

resistance. That is:

$$\begin{aligned} < i^2 > \; &= \; 2qI_bBI_2 \\ &+\frac{2qI_c}{g_m^2}[(\frac{1}{R_B}+\frac{1}{r_\pi})^2BI_2+(2\pi C_t)^2B^3I_3] \\ &+4kTr_b[\frac{BI_2}{R_B^2}+(2\pi)^2(C_d+C_s)^2B^3I_3], \end{aligned} \tag{7}$$

where I_2 and I_3 are integrals whose value depends on the circuit transfer function [22], and B is the bit rate. Also, r_b is the transistor base resistance, and $r_\pi = \beta/g_m$ is the dynamic base resistance. The optical sensitivity is then given by:

$$\bar{P} = (\frac{h\nu}{\eta_{ph}q})Q\langle i^2\rangle^{1/2} \tag{8}$$

where $\bar{P}$, the minimum time-averaged input power required to achieve a given BER, is used instead of P_{min}, and Q is the signal-to-noise ratio for a given BER. For example, $Q = 7$ for BER $= 10^{-12}$. Figure 4 shows the circuit sensitivity as a function of bit rate assuming $I_c = 1mA$ and $10mA$. All the device parameters used in our calculations are listed in Table 1. In most cases, values typical of those reported in the literature for OEICs based on the InP materials system are employed in this analysis. We see that for a given I_c, higher input power ($\bar{P}$) is needed to operate the gate at higher B due to the increase of noise current. Alternatively, $\bar{P}$ is lower for smaller I_c at a given value of B. Therefore it is essential to reduce I_c (and hence I_{th}) in order to improve the optical sensitivity.

We define the detection margin of a logic gate at a given bit rate as the difference between the output power emitted in one stage of a cascade reduced by the interconnection and fanout losses ($P_{out}\eta_c/F$), and the receiver sensitivity of the following stage ($\bar{P}$). Assuming a symmetric current swing, $I_{th} = 1mA$, a laser diode slope efficiency of $0.4mW/mA$, $\eta_c = 0.5$ and $F = 10$, we obtain $P_{out}\eta_c/F = -20dBm$, which corresponds to the upper limit

of the vertical axis in Fig. 4. This results in a detection margin of $15dB$ at $1Gb/s$, which assures the low-noise operation of the system at that bit rate.

To design an interconnection/processing system operating at high bit rate, it is improtant to have a detection margin large enough to maintain the operation of the system at a given BER. From the above results, we conclude that the receiver sensitivity will not significantly affect the performance of OEIC smart pixels operating under the proposed conditions. Since the capacitance of both the photodiode and the transistor contribute significantly to the noise current at high bit rate, the areas of these devices should be minimized, which is also desirable for improving the circuit bandwidth. With a photodiode area of $20 \times 20\mu m^2$ and typical transistor capacitances as listed in Table 1, the optoelectronic NOR gate has a large detection margin which enables it to operate at rates of several gigabits per second.

4 Gain, Bandwidth, and Switching Energy

In a cascaded optical interconnection network, the number of stages allowed is limited by the optoelectronic gain and the optical coupling efficiency between each stage. Gain is required for each interconnect stage to compensate for the coupling losses and to achieve fanout; that is:

$$G \geq F/\eta_c \tag{9}$$

The optoelectronic gain of each interconnect stage is defined by:

$$G = \frac{P_{out}(on)}{P_{in}(on)}, \tag{10}$$

where $P_{in}(on)$ and $P_{out}(on)$ are the input and output optical powers respectively, representing a *logical* "1" *or* "*on*". *For the optoelectronic* NOR gate, the gain can be derived from Eq.(1)

and (2); giving:

$$G = \frac{\eta_{ph}[\eta_d(I_{ld}^{on} - I_{th}) + \eta_{sp} I_{th}]}{2I_{ph}}. \tag{11}$$

where η_{sp} is approximately two orders of magnitude lower than η_d, and hence the last term in Eq.(11) can be neglected. Increasing the current gain (β) of the HBT reduces the I_{ph} needed to turn off the laser diode, thus increasing G. Since the gain-bandwidth product of the circuit is a constant, a high β will also increase r_π, thus decreasing the circuit bandwidth (see below). Figure 5 shows the relationship between F and β for different η_c. We see that $F = 2$ to 20 is obtainable with typical optoelectronic logic gates, although for most switching networks, $F = 2$ to 10 is sufficient.

The frequency response of the optoelectronic NOR gate is determined by the dominant pole of the transfer function. For an accurate frequency response calculation, zero-value time constant analysis [23] can be used, which we present in the Appendix. Since the base resistance, r_b, is much smaller than the dynamic base-emitter resistance $r_\pi = \beta/g_m$, and since $r_\pi \ll R_B$, the total resistance at the input can be approximated by r_π. Thus the bandwidth can be approximated by:

$$\Delta f = \frac{1}{2\pi r_\pi C_t} = \frac{qI_c}{2\pi\beta kTC_t}, \tag{12}$$

where C_t is given by Eq. (6). Figure 6 (solid curves) shows the bandwidth (Δf) of the NOR gate as a function of I_c using the device parameters listed in Table 1. At low I_c, C_π dominates C_t, thus the bandwidth is approximately linear to I_c. As I_c increases, C_M increases and becomes comparable with C_t, and hence the bandwidth curve is flattened. One way to reduce this effect is by using the cascode NOR gate as shown in Fig. 2b (with its equivalent circuit shown in Fig. 3b). The resulting Δf as a function of I_c is plotted by the

dashed curves in Fig. 6. We can see that cascode configuration can improve the bandwidth by as much as 20% in the high collector current region.

Several points should be noted regarding the bandwidth of optoelectronic logic gates. First, although high collector current leads to an increase of the bandwidth, it also increases the noise current in the circuit as discussed in the previous section. Thus the optical sensitivity ultimately determines the bandwidth of the logic gates. Also pixel power dissipation is proportional to the current. Therefore, to design logic gates with high bandwidth, we have to trade off power and speed. Since the gain-bandwidth product of the circuit remains constant for a given I_c, we have to make a compromise between the bandwidth and the optoelectronic gain, and hence between bandwidth and the fanout of the pixel. The latter is reflected by Fig. 7, in which the fanout is plotted against bandwidth for $I_c = 1mA$ and $10mA$, with β as a variable.

Finally, we note that the contribution to C_t from the p-i-n photodiode is area dependent. Although reducing the area of the photodiode improves the bandwidth, it also makes the optical coupling between stages more difficult, thus leading to an increase of input power to compensate for inevitable coupling losses. Figure 8 shows the effect that the area of the photodiode has on the bandwidth for different values of β in both noncascode (solid) and cascode (dashed) circuits assuming $I_c = 1mA$. (The small difference between the cascode and noncascode cases is due to the low I_c as shown by Fig. 6). We see that for a photodiode diameter increase from $5\mu m$ to $15\mu m$, corresponding to a ten-fold increase in area, results in a decrease in Δf from $2GHz$ to $1.5GHz$ (for $\beta = 25$) which is only about 25%. The cause of this relatively weak area dependence of Δf arises since the base-emitter capacitance of the HBT, C_π, is larger than C_d. Hence, the contribution of C_d to C_t is not dominant. This

important result implies that we can make the area of input photodetector larger than that of the HBT to maintain high optical coupling efficiency while still being able to operate the logic gates at high Δf.

The switching energy is defined as the amount of energy change at the input required to switch the gate from one logical state to the other. Thus the switching energy of the optoelectronic NOR gate is given by

$$E_{sw} = \Delta P_{in} \Delta t = [P_{in}(on) - P_{in}(off)]\Delta t. \tag{13}$$

where the switching time is $\Delta t = 1/2\Delta f$, $P_{in}(on)$ is given by Eq.(2), and $P_{in}(off)$ is the input power of logical "0". In a cascaded system, the inputs come from the outputs from the preceding stage. Since $\eta_{sp} \ll \eta_d$, $P_{in}(off)$ is negligible compared with $P_{in}(on)$. Figure 9 shows the switching energy vs bandwidth for an optoelectronic NOR gate. We see that the switching energy increases rapidly with the bandwidth due to the increase in collector current which is needed to raise the gain-bandwidth product of the HBT. Thus for a given current gain, more input optical power is needed to induce a large change of collector current. For $\beta = 100$, for example, the switching energy at a bandwidth of $1GHz$ (corresponding a collector current of $3.5mA$) is about $35fJ$. Note that this value is between one and two orders of magnitude lower than recent experimental data obtained for optoelectronic smart pixels reported in literature. This mainly results from the fact that the circuits have not yet been optimized for high bandwidth operation. For example, HPTs have been used instead of the more advantageous combination of p-i-n diodes and HBT circuits discussed here [6]. Laser diodes with submilliampere threshold as well as high slope efficiency are also required to reduce the switching energy [4]. A listing of recent performance data (including E_{sw}, Δf, etc.) for several different optoelectronic smart pixels is given in Table 2.

5 Power Dissipation and Pixel Packing Density

High density interconnections with a large number of closely spaced pixels are required in numerous high capacity digital system architectures. The maximum pixel packing density (or number of pixels per unit area) of 2-D arrays imposes a limit on the degree of parallelism of the system. One of the constraints on pixel packing density arises from the on-chip power dissipation. For the optoelectronic NOR gate, the optical input power is at least two orders of magnitude less than the electrical power needed to supply the circuit, and hence can be neglected in calculating the maximum, thermal dissipation-limited pixel packing density, ρ. When the laser is on (i.e., for the logical "1"), the power dissipated by the circuit is given by:

$$P_d(on) = V_{cc} I_{ld}^{on} - P_{out}(on) \tag{14}$$

where V_{cc} is the DC supply voltage, and I_{ld}^{on} is the current of the laser diode while it is on. When the laser is off, the power dissipated is:

$$P_d(off) = V_{cc}[I_{ld}^{off} + I_c + I_{ph}] \tag{15}$$

where $P_d(off)$ is due only to spontaneous emission which is negligible compared with the electrical power consumed by the circuit, and I_{ld}^{off} is the laser current in the logical "0" state. Since R_B must be large to achieve a large circuit gain, I_{ph} can be approximated by I_c/β. The average power dissipation of the circuit for a 50% data duty cycle can then be expressed as:

$$P_d = \frac{1}{2}[P_d(on) + P_d(off)]. \tag{16}$$

Figure 10 shows the relationship between power dissipation and I_{th} for two different values of V_{cc} for both the noncascode and cascode circuits. Notice that the larger power dissipation

of cascode circuit is due to the additional amplifier stage which improves the bandwidth of the logic gates. A high threshold current requires a large change in I_c to switch the gate from on to off, thus decreasing the optoelectronic gain of the circuit and increasing the power dissipation. The DC voltage supply, V_{cc}, is predominantly determined by the turn-on voltages of the laser and transistors, which are $\simeq 1V$ each. To reduce the power dissipation of the circuit, a small V_{cc} is desirable. HBTs based on InGaAs/InP have turn-on voltages of $0.75V$[26] whereas GaAs/AlGaAs HBTs have turn-on voltage of $1.43V$ due to the larger bandgap of GaAs [26]. These low turn-on voltages allow the logic gates to operate at high speed from a supply voltage of from $3V$ (for InGaAs/InP) to $5V$ (for AlGaAs/GaAs), corresponding to a power dissipation of 4 to $8mW$ per pixel assuming $I_{th} = 1mA$. If we assume the maximum thermal power that can be dissipated by a chip is $1W/cm^2$ as is typical for silicon VLSI circuits using passive cooling, then the maximum pixel packing density (ρ) is between 150 and $250cm^{-2}$ for the noncascode circuit, and between 100 and $170cm^{-2}$ for the cascode case, as shown in Fig. 11. Although a large collector current swing will increase the bandwidth as described above, the pixel packing density decreases rapidly with the increase in current. Arrays with pixel densities such as these are known as a "medium grained".

6 Temperature Sensitivity

The major source of thermal sensitivity in optoelectronic logic gates comes from the temperature dependence of the threshold current of the laser diode, which is described by the empirical expression

$$I_{th}(T) = I_0 exp(T/T_0) \tag{17}$$

where T_0 is a characteristic temperature associated with the laser material and device design. Under cw operation at room temperature, the power dissipated by the laser will raise the temperature, and thus the threshold current. To maintain constant output power, more laser current is required, thus increasing the temperature still further. Typical values of T_0 are 120K and 200K for double heterostructure (DH) and multiple quantum well (MQW) GaAs/AlGaAs lasers operating at $\lambda = 0.8\mu m$, respectively, and 50-70K for both bulk-active DH and MQW InGaAsP/InP lasers operating in the wavelength range of $\lambda = 1.3 - 1.55\mu m$. Recent progress has increased T_0 close to 100K in strained quantum lasers[15]. Assuming a laser diode with a $T_0 = 70K$ has a threshold $I_{th} = 1mA$ at $T = 293K$, then the maximum temperature of the system determines the threshold current, which in turn gives the maximum possible pixel packing density. This is calculated in Fig. 12. We can see that as the system temperature rises, the maximum allowed pixel packing density decreases rapidly. With $T_0 = 150K$, the dependence of pixel packing density on temperature is less than for $T_0 = 70K$. Thus, higher T_0 reduces the temperature sensitivity of optoelectronic logic circuits.

7 Sensitivity to Variations in Laser Threshold Current

In a system with large arrays, variations in laser threshold current from pixel to pixel need to be small in order to switch the lasers with the same input light intensity. However, in practical arrays, the laser threshold current will differ from pixel to pixel due to variations in device fabrication, operating environment (temperature, etc.), and other changes in system or device characteristics. The immediate effect of a variation in laser threshold current is a variation of optoelectronic gain, G, from pixel to pixel. The variation of G limits the

maximum fanout, F, given the relationship between G and F in Eq. (9). Thus the input power to the second stage in a cascaded network will deviate from the desired level. This deviation at the input can cause, in the worst case, a failure of the second stage.

The variation of laser threshold current can be expressed by $\Delta I_{th}/I_{th0} = [I_{th} - I_{th0}]/I_{th0}$. Figure 13 shows the effect of threshold current fluctuations (given by $\Delta I_{th}/I_{th0}$) on the optoelectronic gain of the logic gate for different slope efficiencies of the laser diode. We can see that a 10% fluctuation of I_{th} can change G and F by a factor of 2 to 3. The effect of variation of slope efficiency also changes G and F proportionally as shown by Fig. 13. These results suggest tight control of device variation during fabrication is necessary for consistent system performance of optoelectronic-based logic pixels.

8 Conclusions

We have analyzed an optoelectronic NOR gate for the purpose of comparing different smart pixel technologies. Our results show that smart pixels based on optoelectronic circuits can have a typical optical sensitivity of $-35dBm$ at bit rates greater than $1Gb/s$ and at BER= 10^{-12}, which leaves a detector margin of $15dB$ for the minimum required input power per logic gate. Bandwidths of such gates exceed $1GHz$ for transistor collector currents in the several milliampere range. Also the bandwidth does not strongly depend on the area of the photodiode, which is advantageous for improving the optical coupling efficiency by using a photodetector with a large photosensitive area. Switching energies of tens of femtojoules at $1GHz$ bandwidth are possible using submilliampere threshold, high efficiency laser diodes. Pixel packing density is ultimately limited by thermal dissipation to a value of $\simeq 200/cm^2$ for a total chip power dissipation of $1W/cm^2$, although the packing density

can be increased at bandwidths below $1GHz$. The temperature dependence of the laser threshold causes moderate temperature sensitivity of the logic gates. Furthermore we note that optoelectronic logic gates are insensitive to wavelength since the photodetector spectral sensitivity is extremely broad. Hence, as the temperature of the pixel array varies (due to power dissipation or environmental fluctuations), the laser emission wavelength will shift, although this will have negligible effect on the overall system performance (if we ignore difficulties and constraints which this shift imposes on the interstage interconnection optics). This insensitivity to wavelength is advantageous as compared with SEED-based logic gates which require operation near the semiconductor band edge. As will be shown in the subsequent paper, this operation near the band edge imposes a serious limitation to SEED-based array stability with temperature. We will present the analysis of SEED-based smart pixel technology and compare these two different approaches in Paper II.

Finally, although this point will be discussed in greater depth in Paper II, a figure of merit useful for characterizing 2D pixel arrays is the information flux density, $\mathcal{F} = \Delta f \rho$. That is, $\mathcal{F}$ represents the maximum data capacity of a system consisting of such smart pixel arrays. From the above discussion, we see that for optoelectronic gates at $\Delta f = 1GHz$, ρ is approximately $200/cm^2$ at a chip power dissipation of $1W/cm^2$. This results in $\mathcal{F} \simeq 200GHz/cm^2$ (which is proportaional to chip power dissipation), which is roughly one to two orders of magnitude higher than calculated for SEED-based pixels arrays (see Paper II).

Acknowledgments

The authors thank the Air Force Office of Scientific Research (A. Craig), Rome Air Development Center/Hanscom Air Force Base (J. Lorenzo), and Siemens Corporate Research for partial support of this work.

Appendix: Bandwidth Calculation

The frequency response of a wideband integrated circuit can be analyzed by deriving the transfer function for the small-signal equivalent of the circuit. If the transfer function contains only poles and no zeros, and if there exists a dominant pole, the gain magnitude can then be given by [23] :

$$|A(j\omega)| \simeq \frac{K}{\sqrt{1+(\omega/p_1)^2}}, \tag{18}$$

where ω is the angular frequency, $A(j\omega)$ is the frequency-dependent small signal voltage transfer function, K is the constant low frequency gain, and p_1 is the dominant pole of $A(j\omega)$. When $\omega = |p_1|$, the gain magnitude decreases to $-3dB$ of its low frequency value. Therefore, the bandwidth $(3dB)$ is given by:

$$\Delta f = \omega_{3dB}/(2\pi) = |p_1|/(2\pi) = 1/(2\pi b_1), \tag{19}$$

where b_1 is a time constant.

To calculate the dominant pole of the circuits shown in Fig. 2 (a) and (b), we apply zero-value time constant analysis [23] to their equivalent circuits shown in Fig. 3 (a) and (b). For Fig. 3(a), in the case of single-stage amplifier, we first evaluate the driving-point resistance at each capacitance node pair with all capacitances put equal to zero. This is given by:

$$R_{d0} = R_B \parallel (r_b + r_\pi), \tag{20}$$

Similarly, we can obtain $R_{\pi 0}$ at the C_π node pair:

$$R_{\pi 0} = r_\pi \parallel (r_b + R_B); \tag{21}$$

and $R_{\mu 0}$ at the $C_{\mu 0}$ node pair:

$$R_{\mu 0} = R_{\pi 0} + R_L \parallel R_{ld} + g_m R_{\pi 0}(R_L \parallel R_{ld}), \tag{22}$$

The zero-value time constant is then given by:

$$b_1 = R_{d0}(C_d + C_s) + R_{\pi 0} C_\pi + R_{\mu 0} C_\mu. \tag{23}$$

Using Eq. (17), the bandwidth of the gate is obtained as:

$$\Delta f = \frac{1}{2\pi [R_{d0}(C_d + C_s) + R_{\pi 0} C_\pi + R_{\mu 0} C_\mu]}. \tag{24}$$

In our particular case, $R_B \gg r_\pi \gg r_b$ and $r_\pi \gg (R_L \parallel R_{ld})$, which gives $R_{d0} \simeq r_\pi \simeq R_{\pi 0}$, and $R_{\mu 0} \simeq r_\pi [1 + g_m(R_L \parallel R_{ld})]$. Thus the bandwidth is given by:

$$\Delta f = \frac{1}{2\pi r_\pi (C_d + C_s + C_\pi + C_M)}, \tag{25}$$

where $C_M = C_\mu [1 + g_m(R_L \parallel R_{ld})]$. This result can also be obtained by using the Miller approximation.

For the case of cascode configuration as shown by Fig. 2b, its equivalent circuit is shown by Fig. 3b. Now there are two more capacitors, $C_{\pi 3}$ and $C_{\mu 3}$, due to the addition of the common-base transistor. Using zero-value time constant analysis, the driving-point resistance at each capacitance node pair is evaluated assuming the the transistors are identical:

$$R_{d0} = R_B \parallel (r_b + r_\pi) \tag{26}$$

$$R_{\pi 01} = r_\pi \parallel (r_b + R_B) \tag{27}$$

$$R_{\mu 01} = R_\pi + R_{i3} + g_m R_{\pi 01} R_{i3} \tag{28}$$

$$R_{\pi 03} = r_\pi \parallel (1/g_m) \tag{29}$$

$$R_{\mu 03} = r_b + (R_L \parallel R_{ld}) \tag{30}$$

where $R_{i3} = [1/g_m + r_b/(\beta + 1)]$. The bandwidth is then given by:

$$\Delta f = \frac{1}{2\pi[R_{d0}(C_d + C_s) + R_{\pi 01}C_{\pi 1} + R_{\mu 01}C_{\mu 1} + R_{\pi 03}C_{\pi 3} + R_{\mu 03}C_{\mu 3}]}. \tag{31}$$

Using Eq. (22) and (29), we calculated the bandwidth of the circuit for both the single-stage and the cascode cases, as shown in Fig. 6. We can see that at high collector current, the cascode circuit shows improved bandwidth. If high bandwidth is of ultimate importance, cascode designs should be used at the cost of increased drive current and power dissipation.

References

[1] J. W. Goodman, F. I. Leonberger, Sun-Yuan Kung, and R. A. Athale, "Optical interconnections for VLSI systems," Proc. IEEE, vol. 72, pp. 850-866, 1984.

[2] H. S. Hinton, "Architectural considerations for photonic switching networks," IEEE J. Sel. Areas Com., vol. 6, pp. 1209-1226, 1988.

[3] J. E. Midwinter, "Photonic switching technology: Component characteristics versus network requirements," J. Lightwave Technol., vol. 6, pp. 1512-1519, 1988.

[4] G. R. Olbright, R. P. Bryan, K. Lear, T. M. Brennan, G. Poirier, Y. H. Lee, and J. L. Jewell, "Cascadable laser logic devices: Discrete integration of phototransistors with surface-emitting laser diodes," Electron. Lett., vol. 27, pp. 216-217, 1991.

[5] P. Zhou, J. Cheng, C. F. Schaus, S. Z. Sun, C. Hains, K. Zheng, E. Armour, W. Hsin, D. R. Myers, and G. A. Vawter, "Cascadable, latching photonic switch with high optical gain by the monolithic integration of vertical-cavity surface-emitting laser and a pn-pn photothyristor," IEEE Photon. Technol Lett., vol. 3, pp. 1009-1012, 1991.

[6] J. J. Brown, J. T. Gardner, S. R. Forrest, "Optically powered, integrated 'smart' pixels for optical interconnection networks," IEEE Photon. Technol Lett., vol. 3, pp. 1136-1138, 1991.

[7] A. L. Lentine, H. S. Hinton, D. A. B. Miller, J. E. Henry, J. E. Cunningham, and L. M. Chirovsky, "Symmetric self-electrooptic effect device: Optical set-reset latch, differential modulator/detector," IEEE J. Quantum Electron., vol. 25, pp. 1928-1936, 1989.

[8] D. A. B. Miller, "Quantum well self electro-optic effect devices," Opt. and Quantum Electron., vol. 22, pp. S61-S98, 1990.

[9] M. G. Taylor and J. E. Midwinter, "Optically interconnected switching networks," J. Lightwave Technol., vol. 9, pp. 791-798, 1991.

[10] L. Cheng and A. A. Sawchuk, "Three-dimensional Omega networks for optical implementation," Appl. Optics, vol. 31, pp. 5468-5479, 1992.

[11] K. Y. Lau, P. L. Derry, and A. Yariv, "Ultimate limit in low-threshold quantum well GaAlAs semiconductor lasers," Appl. Phys. Lett., vol. 52, pp. 88-90,1988.

[12] R. S. Geels, S. W. Corzine, and L. A. Coldren, "InGaAs vertical-cavity surface-emitting lasers," IEEE J. Quantum Electron., vol. 27, pp. 1359-1367, 1990.

[13] H. Temkin, N. K. Dutta, T. Tanbun-Ek, R. A. Logan, and A. M. Sergent, "InGaAs/InP quantum well lasers with sub-mA threshold current," Appl. Phys. Lett., vol. 56, pp. 1610-1612, 1990.

[14] C. E. Zah, F. J. Favire, S. G. Menocal, N. C. Andreadakis, D. M. Hwang, M. Koza, and T. P. Lee, "Submilliampere-threshold 1.5 μm strained layer multiple quantum well lasers," IEEE Photon. Technol Lett., vol. 2, pp. 852-853, 1990.

[15] P. J. A. Thijs, L. F. Tiermeijer, P. I. Kuindersma, J. J. M. Binsma, and T. Van Dongen, " High-performance 1.5μm wavelength InGaAs/InGaAsP strained quantum well lasers and amplifiers," IEEE J. Quantum Electron., vol. 27, pp. 1426-1439, 1991.

[16] M. Govindarajan and S. R. Forrest, "Design considerations for wideband p-i-n/HBT monolithic transimpedance optical receivers," J. Lightwave Technol., in press (Feb., 1993).

[17] S. J. Kim, G. Guth, G. P. Vella-Colerio, C. W. Seabury, W. A. Sponsler, and B. J. Rhoades, "Monolithic integration of InGaAs p-i-n photodetector with fully implanted InP JFET amplifier," IEEE Electron Device Lett., vol. 9, pp. 447-449, 1988.

[18] D. C. W. Lo, Y. K. Chung, S. R. Forrest, "A high performance monolithic InGaAs voltage-tunable transimpedance amplifier," IEEE Photon. Technol Lett., vol. 2, pp. 675-677, 1990.

[19] S. Chandrasekhar, B. C. Johnson, E. Tokumitsu, A. G. Dentai, C. H. Joyner, A. H. Gnauck, J. S. Perino, and G. J. Qua, "A monolithic long wavelength photoreceiver using heterojunction bipolar transistors," IEEE J. Quantum Electron., vol. 27, pp. 773-777, 1991.

[20] L. Y. Leu, J. T. Gardner, and S. R. Forrest, "A high sensitivity InGaAs/InP heterojunction phototransistor," Appl. Phys. Lett., vol. 57, pp. 1251-1253, 1990.

[21] S. R. Forrest, "Performance of InGaAsP photodiodes with dark current limited by diffusion, generation recombination, and tunneling," IEEE J. Quantum Electron. , vol. 17, pp. 217-226, 1981.

[22] R. G. Smith and S. D. Personick, "Receiver Design for Optical Fiber Communications," Chap. 4, in *Semiconductor Devices for Optical Communication*, ed. H. Kressel, New York: Springer-Verlag, 1982.

[23] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, New York: Wiley, 2nd ed., 1984.

[24] S. R. Forrest, "Optical Detectors for Lightwave Communication", in *Optical Fiber Telecommunications II*, Boston: Academic Press, 1988.

[25] Yue Liu, Ph. D. Dissertation, University of Southern California, 1991

[26] B. Jalali and R. N. Nottenburg, "Heterostructure Bipolar Transistors", Chap. 12, in *Indium Phosphide and Related Materials: Processing, Technology, and Devices*, ed. A. Katz, Boston: Artech House, 1992.

[27] K. Kasahara, "VSTEP-based smart pixels", IEEE J. Quantum Electron., vol. 29, pp. 757-768, 1993.

Figure Captions

Figure 1: Schematic optical interconnection and information processing systems using source (a) or modulator (b).

Figure 2: Schematic circuit diagrams of an optoelectronic NOR gate with (a) single-stage amplifier; (b) cascode.

Figure 3: Small-signal equivalent circuits of the optoelectronic NOR gates in Fig. 2: (a) single-stage amplifier; (b) cascode.

Figure 4: Receiver sensitivity ($\bar{P}$) as a function of system bit rate (B) for two different collector currents (I_c). Note the gate dynamic range (D. R.) for $I_c = 1mA$ is $\sim 15dB$ at $B = 1Gb/s$.

Figure 5: Fanout (F) of the optoelectronic NOR gate as a function of HBT current gain (β) for three values of coupling efficiency (η_c).

Figure 6: Bandwidth (Δf) of the optoelectronic NOR gate as a function of collector current (I_c) of the HBT. The solid curves correspond to single-stage amplifiers (as in Fig. 2a) and the dashed curves for cascode circuits (Fig. 2b).

Figure 7 : Fanout (F) of the optoelectronic NOR gate as a function of bandwidth (Δf) assuming the p-i-n diode area is $20 \times 20\mu m^2$. The solid curve corresponds to $I_c = 1mA$ and dashed curve to $I_c = 10mA$.

Figure 8: The effect of p-i-n photodiode diameter on bandwidth (Δf) plotted for three values of HBT current gain (β) of the optoelectronic NOR gate, assuming the collector current is $1mA$. The solid curve corresponds to the noncascode circuit, and the dashed curve to the cascode circuit.

Figure 9: Logic gate switching energy (E_{sw}) as a function of the bandwidth (Δf) for three values of HBT current gain (β).

Figure 10: Power dissipation (P_d) of the optoelectronic NOR gate as a function of laser threshold current (I_{th}) for a given power supply voltage (V_{cc}). Typically, $P_d \simeq 5mW$ for $I_{th} = 1mA$, representing a practical minimum power dissipation anticipated for optoeletronic-based bipolar smart pixels. The solid curve corresponds to the noncascode circuit, and the dashed curve to the cascode circuit.

Figure 11: Pixel packing density (ρ) of the optoelectronic NOR gate as a function of the laser threshold current (I_{th}) assuming the maximum total thermal power density that can be dissipated by a chip is $1W/cm^2$. The solid curve corresponds to the noncascode circuit, and the dashed curve to the cascode circuit.

Figure 12: Effects of system temperature on the pixel packing density of optoelectronic NOR gates assuming $I_{th} = 1mA$ at $T = 293K$. The solid curves correspond to $T_0 = 70K$ (typical of InP-based technology) and the dashed curves correspond to $T_0 = 150K$ (typical of GaAs-based OEIC gates).

Figure 13: Effects of variations of laser threshold current and slope efficiency on the optoelectronic gain, G, assuming $I_{th0} = 1mA$.

Table 1 Parameters of the Optoelectronic NOR Gate

Capacitance of p-i-n diode (20μmx20μm)	C_d	40 fF
Stray capacitance	C_s	40 fF
Base-emitter capacitance(5μmx5μm)	C_π	100 fF
Base-collector junction capacitance(5μmx5μmx0.5μm)	C_μ	5 fF
Miller capacitance	C_M	$C_{bc}(1+g_m R_L \| R_{ld})$
Current gain	β_0	100
Transconductance	g_m	qI_c/kT
Dynamic base-emitter resistance	r_{be}	β_0/g_m
p-i-n bias resistance	R_B	20 kΩ
Combined load resistance	$R_L \| R_{ld}$	50 Ω

Table 2 Performance of Optoelectronic Smart Pixels

	Brown (1991)	Olbright(1991)	Kasahara(1993)	Zhou(1991)
Reference	[6]	[4]	[27]	[5]
Detector/Source	HPT/LD	HPT/LD	VSTEP	HPT/LD
Materials	InGaAs/InP	AlGaAs/GaAs	AlGaAs/GaAs	AlGaAs/GaAs
Wavelength(μm)	1.3	0.85	0.95	0.83
Bias Voltage (V)	3.8	8	6.1	3
Current(mA)	22	10	8.5	5
Bandwidth(MHz)	30	2	100	2
Gain	100	2700	10	1000
Contrast Ratio	11	20	>1000	$3x10^4$
Switching Energy(pJ)	3.8	1	2.5	6
Power Dissipation per pixel (mW)	81	80	50	15

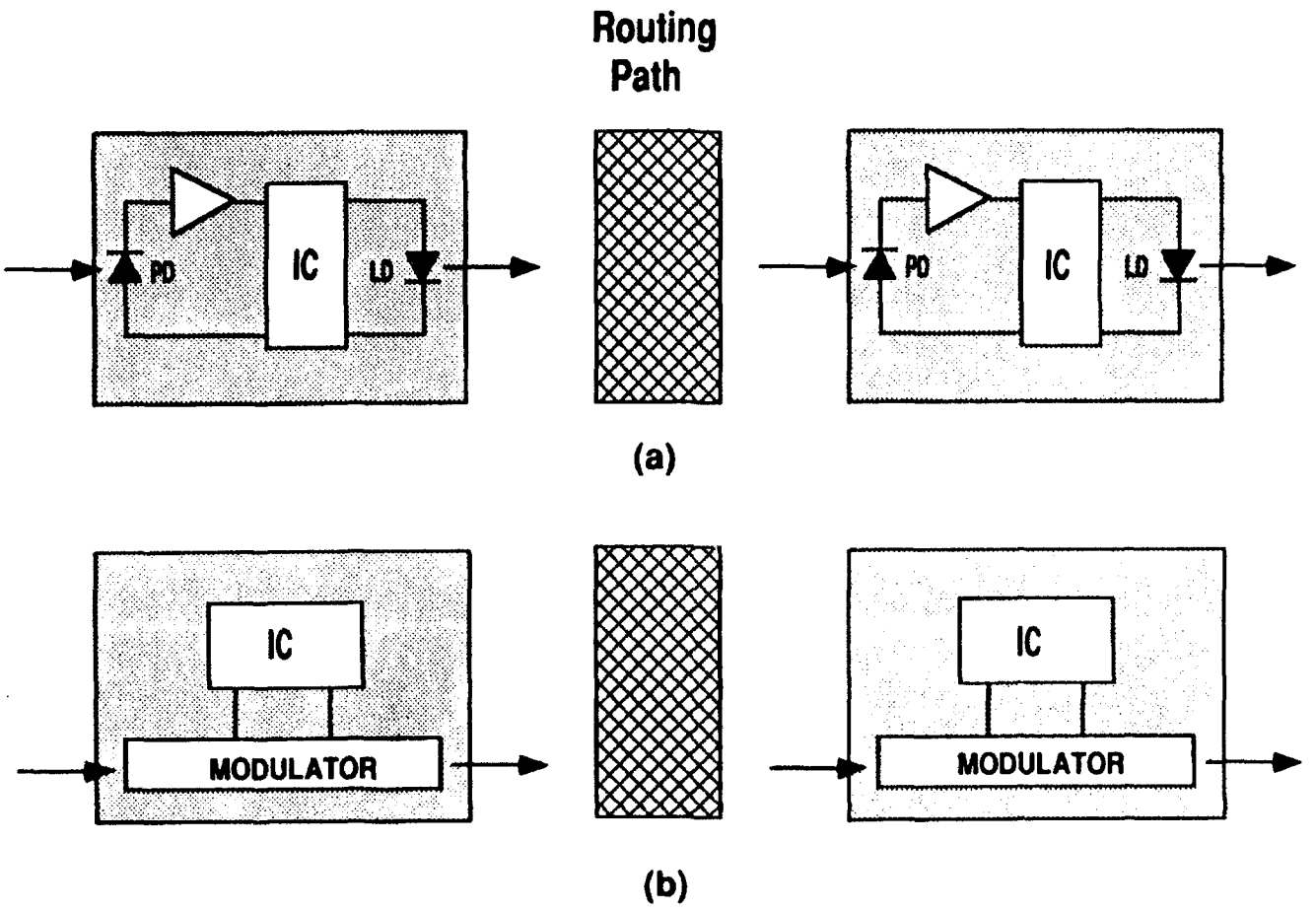
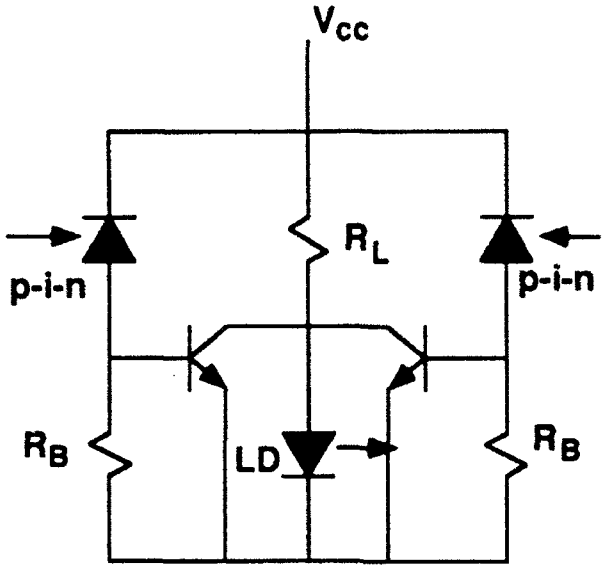
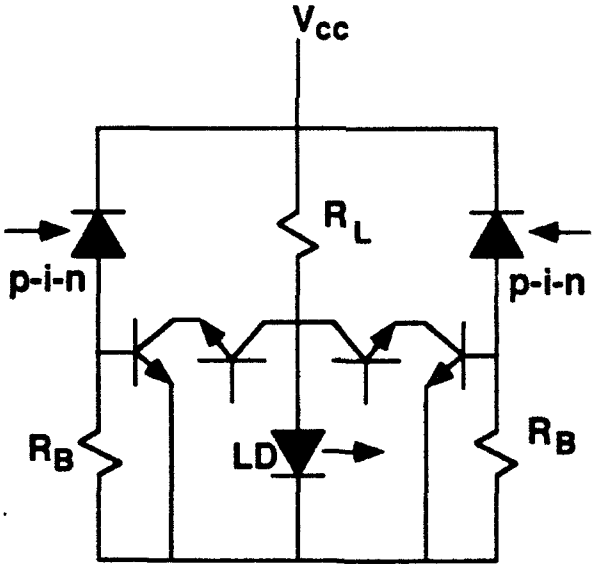


Fig. 1

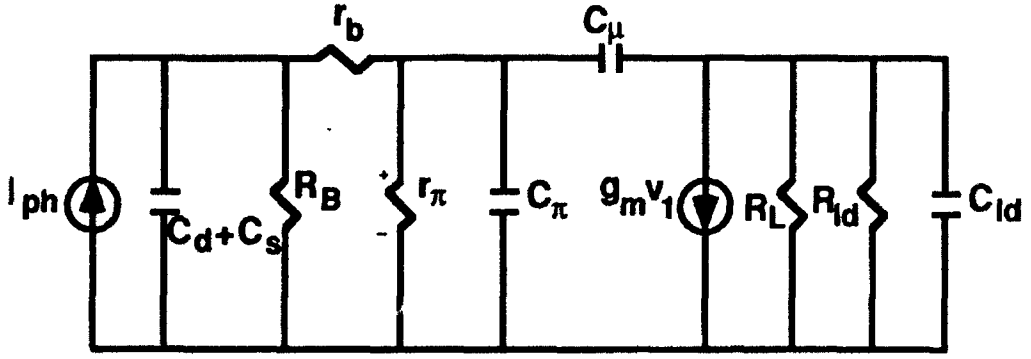


(a)

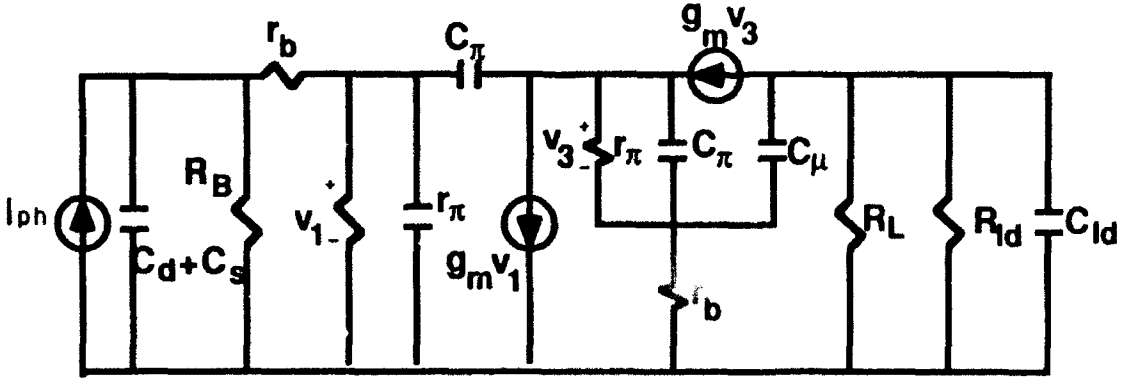


(b)

Fig. 2


r_b
C_μ
I_{ph}
C_d+C_s
R_B
r_π
C_π
$g_m v_1$
R_L
R_{ld}
C_{ld}

(a)


r_b
C_π
$g_m v_3$
v_3
r_π
C_π
C_μ
R_B
I_{ph}
v_1
r_π
C_d+C_s
$g_m v_1$
i_b
R_L
R_{ld}
C_{ld}

(b)

Fig. 3

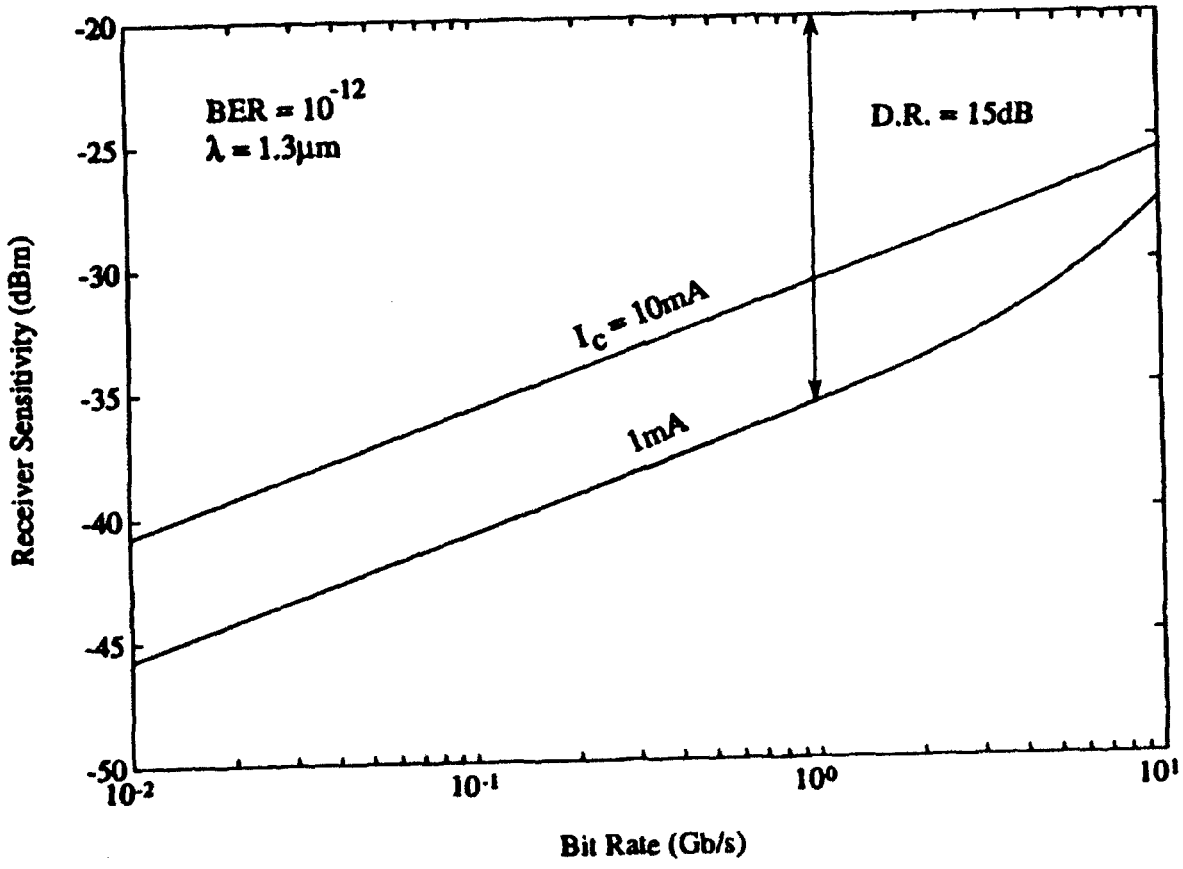

BER = 10^{-12}
λ = 1.3μm
D.R. = 15dB
I_c = 10mA
1mA
Receiver Sensitivity (dBm)
-20
-25
-30
-35
-40
-45
-50
10^{-2}
10^{-1}
10^{0}
10^{1}
Bit Rate (Gb/s)

Fig. 4.

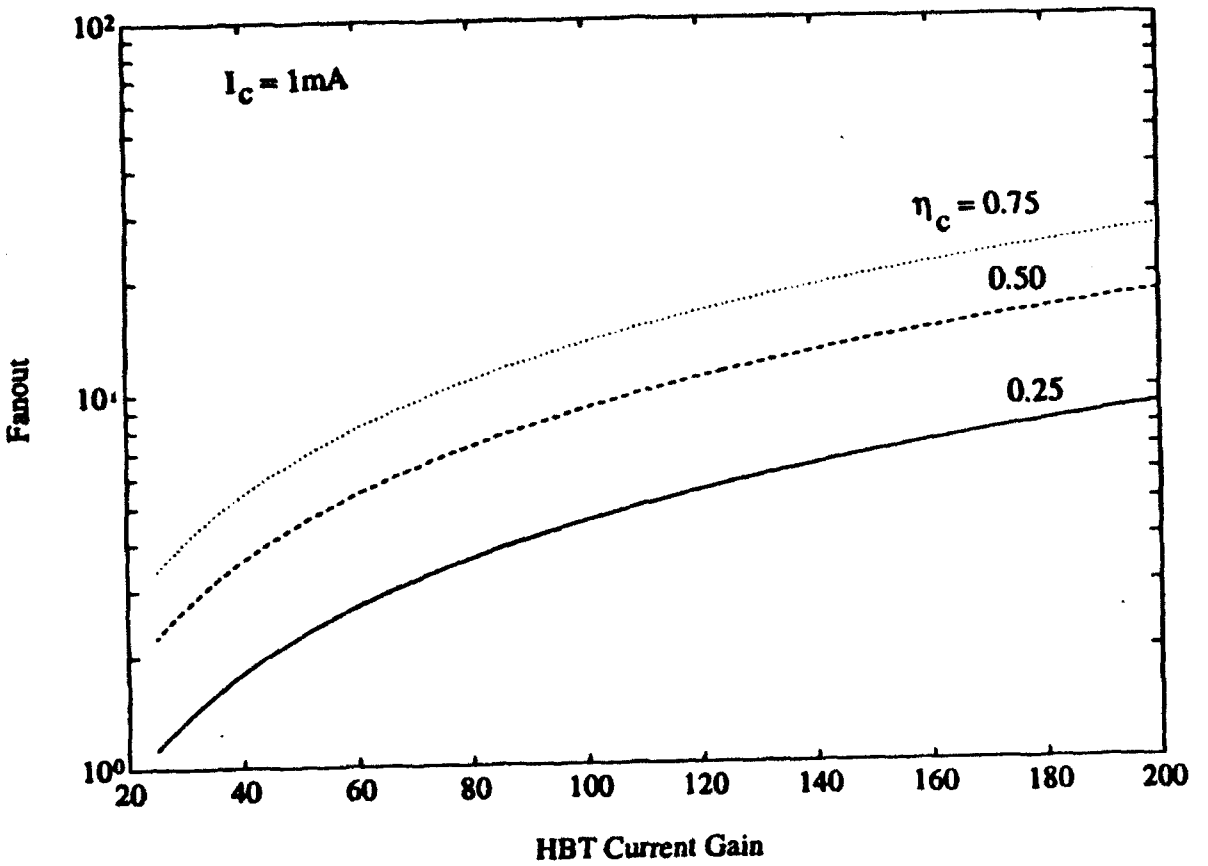
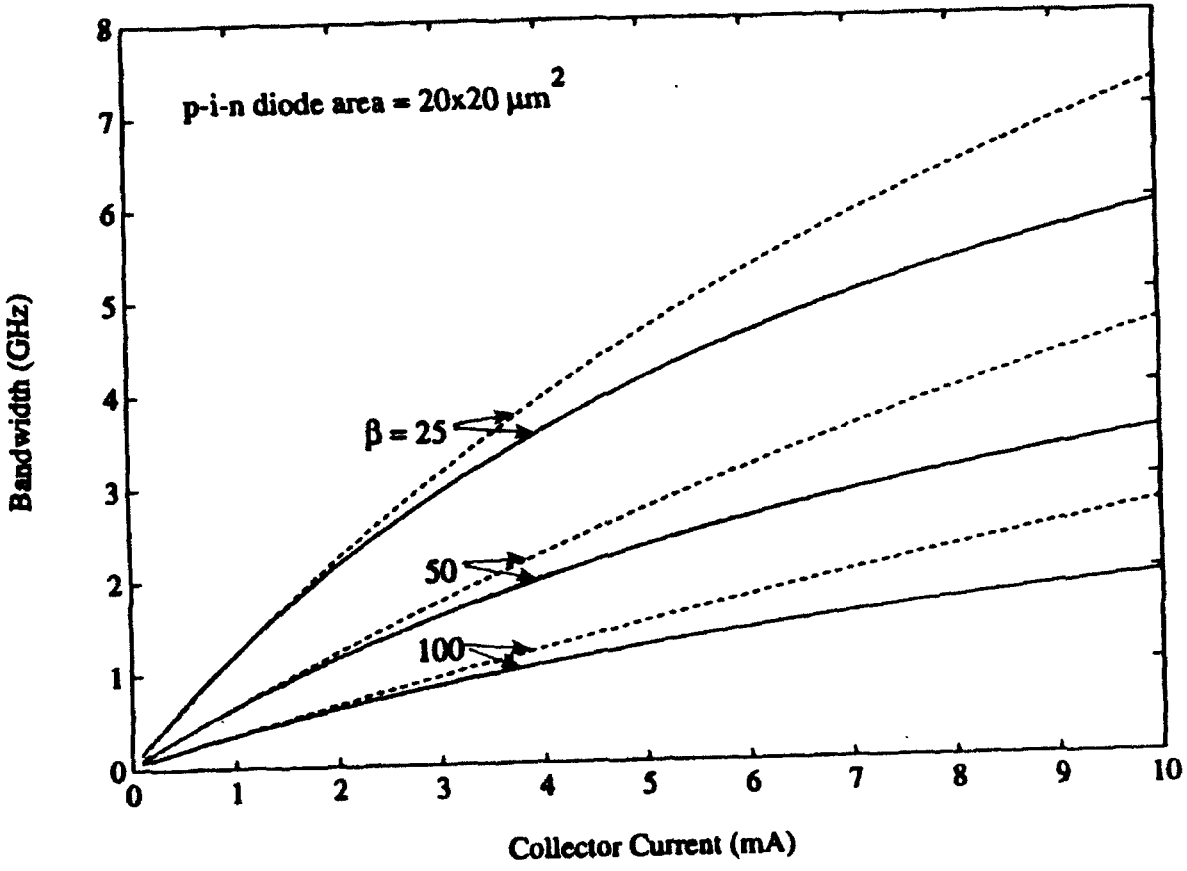

10^2
10^1
10^0
$I_c = 1mA$
$\eta_c = 0.75$
0.50
0.25
Fanout
20
40
60
80
100
120
140
160
180
200
HBT Current Gain

Fig 5


p-i-n diode area = 20x20 μm²
β = 25
50
100
Bandwidth (GHz)
Collector Current (mA)
0
1
2
3
4
5
6
7
8
9
10

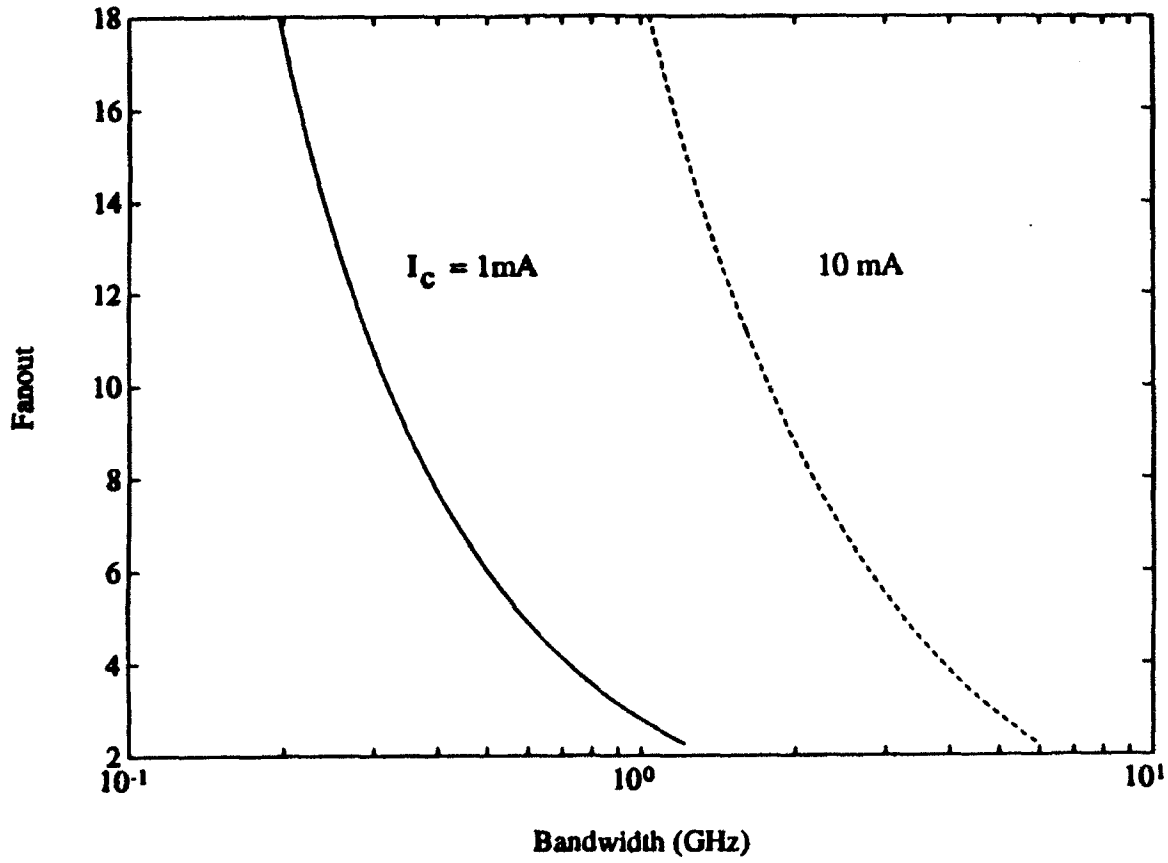

18
16
14
12
10
8
6
4
2
Fanout
I_c = 1mA
10 mA
10^{-1}
10^0
10^1
Bandwidth (GHz)

Fig 7

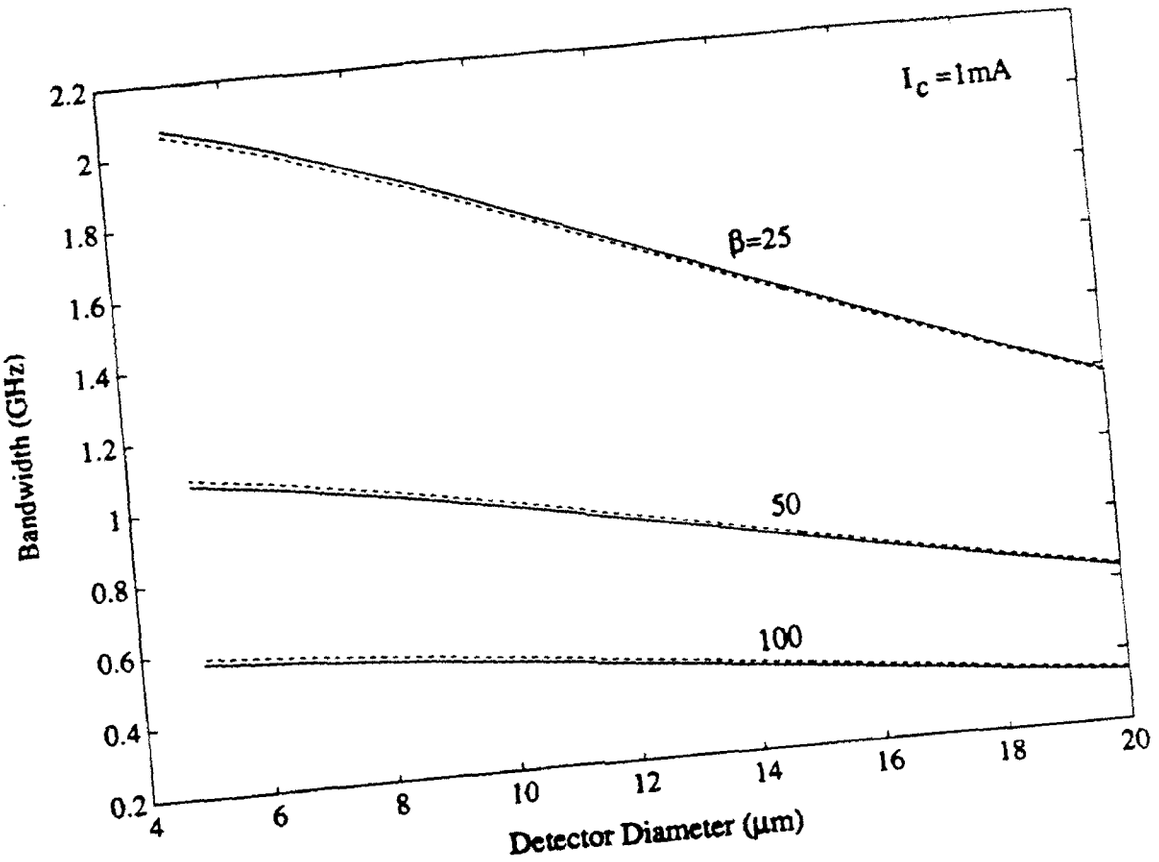

I_c =1mA
β=25
50
100
Bandwidth (GHz)
Detector Diameter (μm)
2.2
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
4
6
8
10
12
14
16
18
20

Fig. 8

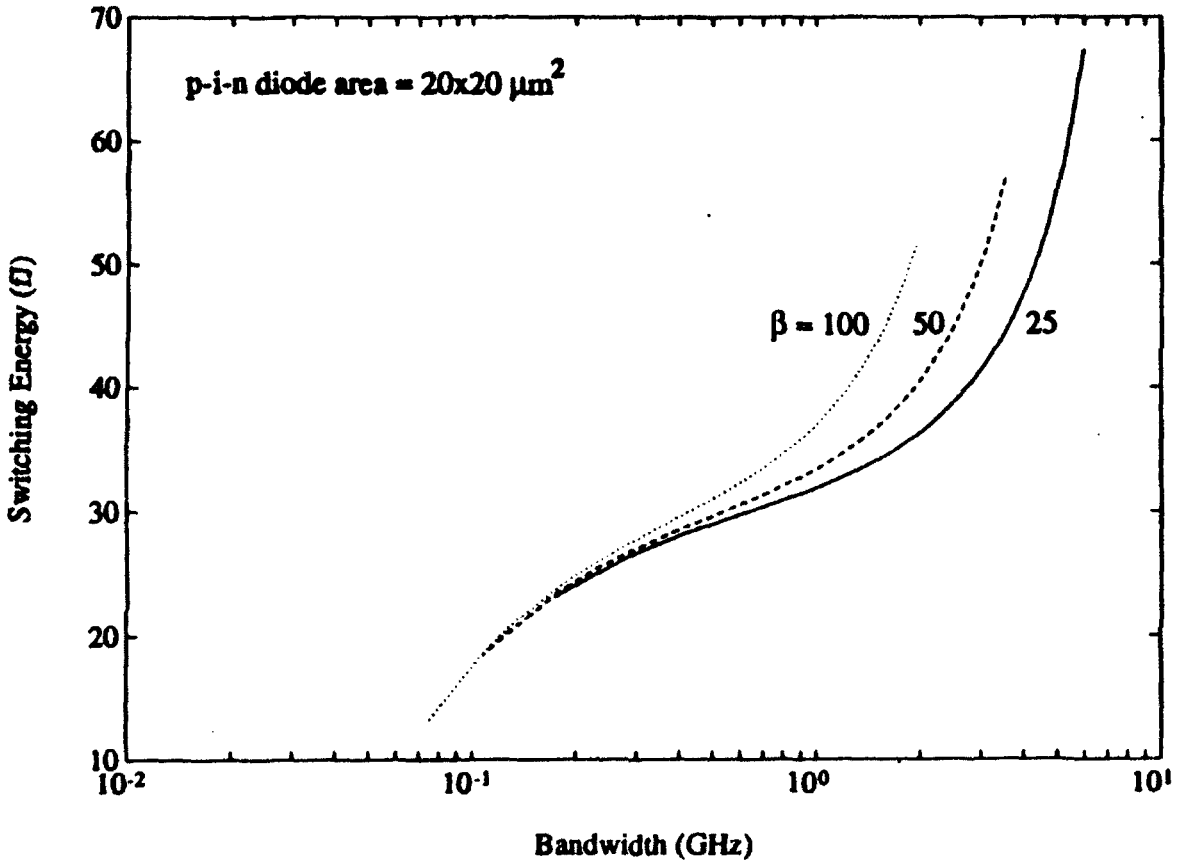

p-i-n diode area = 20x20 μm²
β = 100
50
25
Switching Energy (fJ)
Bandwidth (GHz)
70
60
50
40
30
20
10
10⁻²
10⁻¹
10⁰
10¹

Fig 9

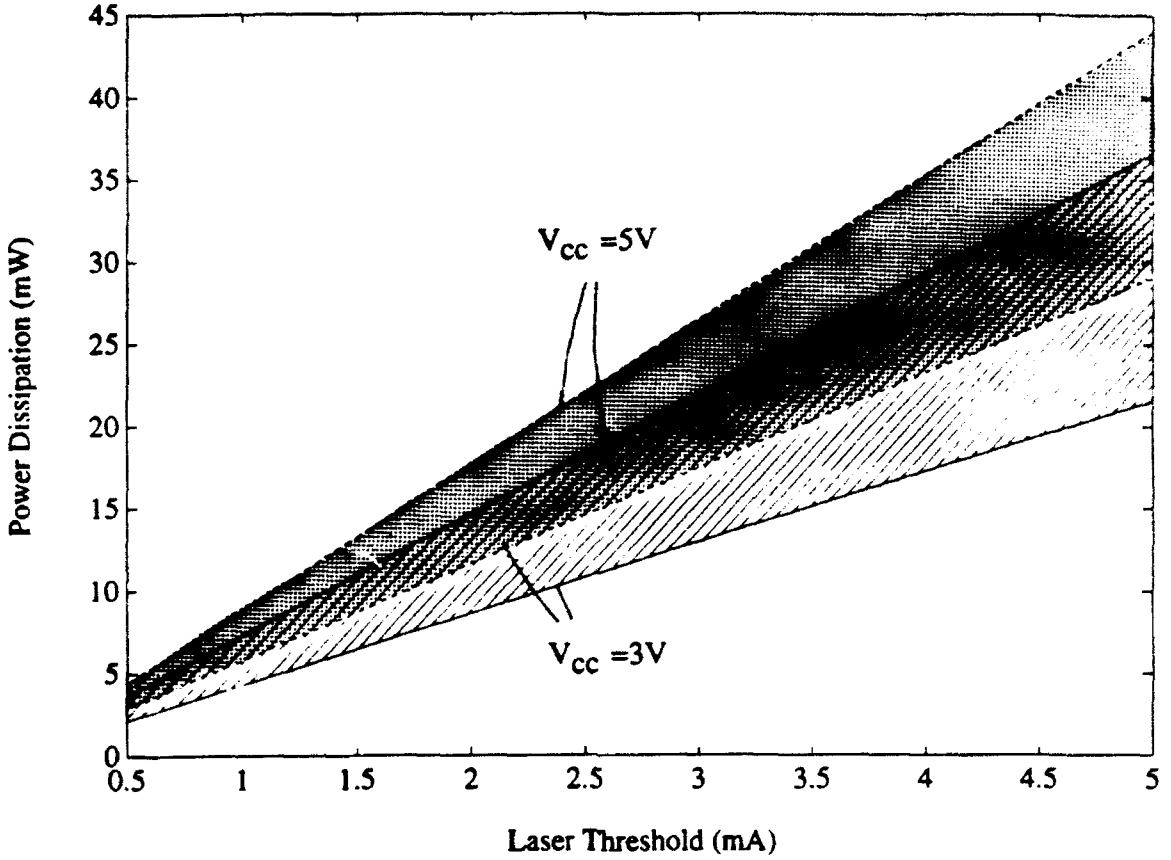

Power Dissipation (mW)
45
40
35
30
25
20
15
10
5
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Laser Threshold (mA)
V_{cc} =5V
V_{cc} =3V

Fig 10

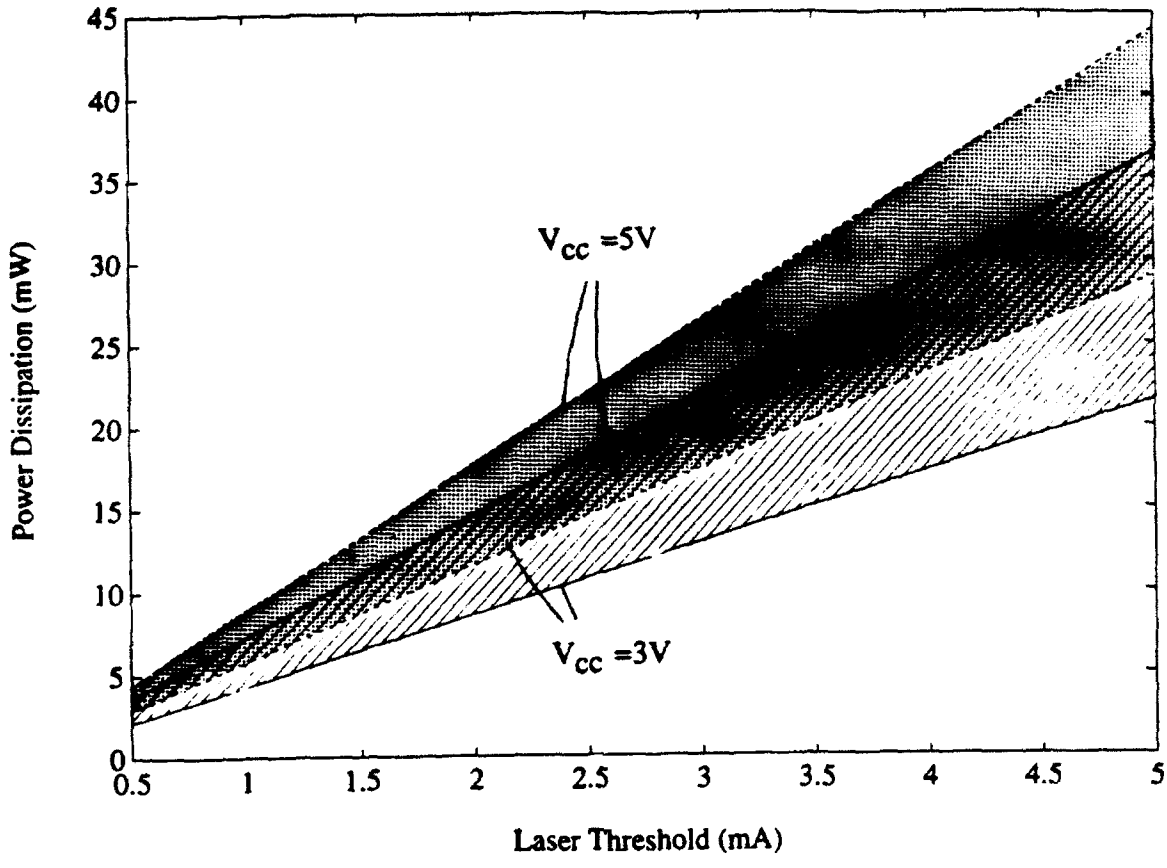

45
40
35
30
25
20
15
10
5
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Power Dissipation (mW)
Laser Threshold (mA)
V_{cc} =5V
V_{cc} =3V

Fig. 10

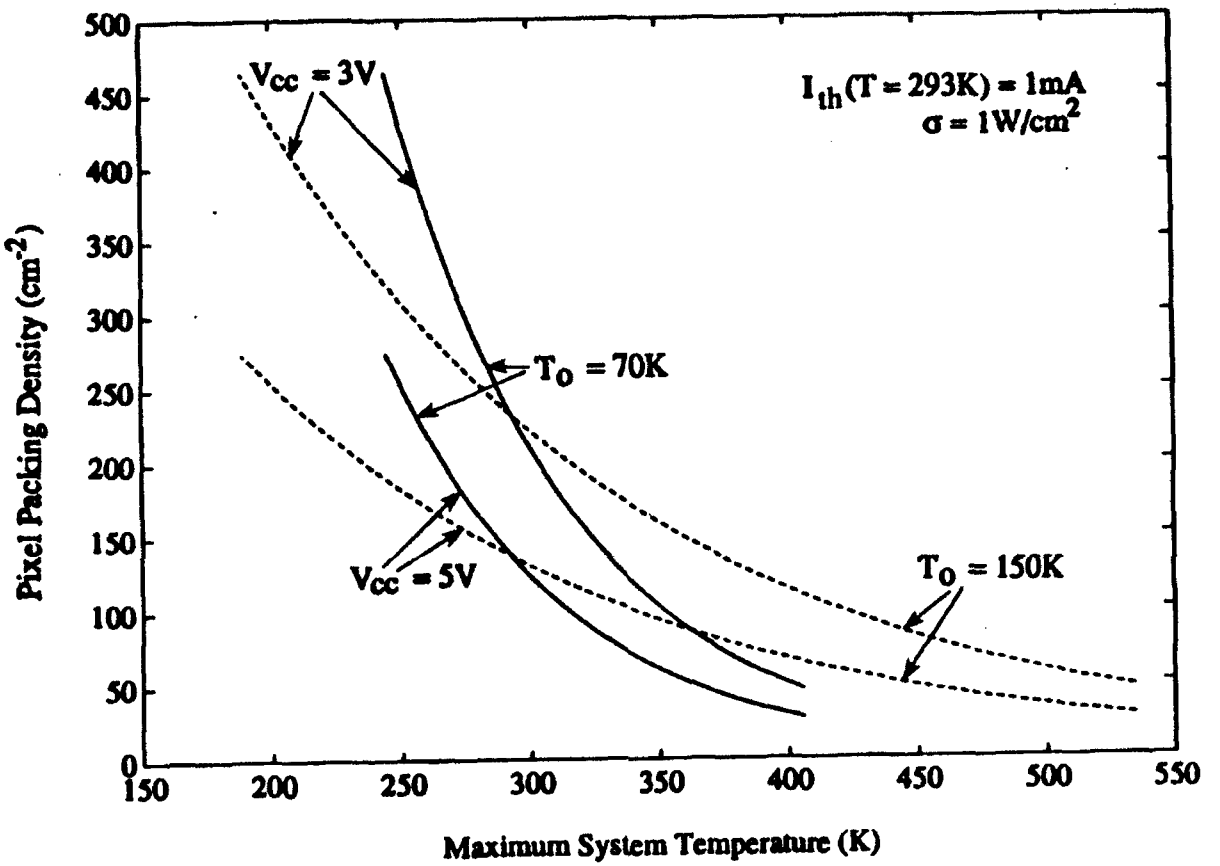

Pixel Packing Density (cm^{-2})
Maximum System Temperature (K)
$I_{th}(T = 293K) = 1mA$
$\sigma = 1W/cm^2$
$V_{cc} = 3V$
$V_{cc} = 5V$
$T_o = 70K$
$T_o = 150K$
0
50
100
150
200
250
300
350
400
450
500
150
200
250
300
350
400
450
500
550

Fig. 12

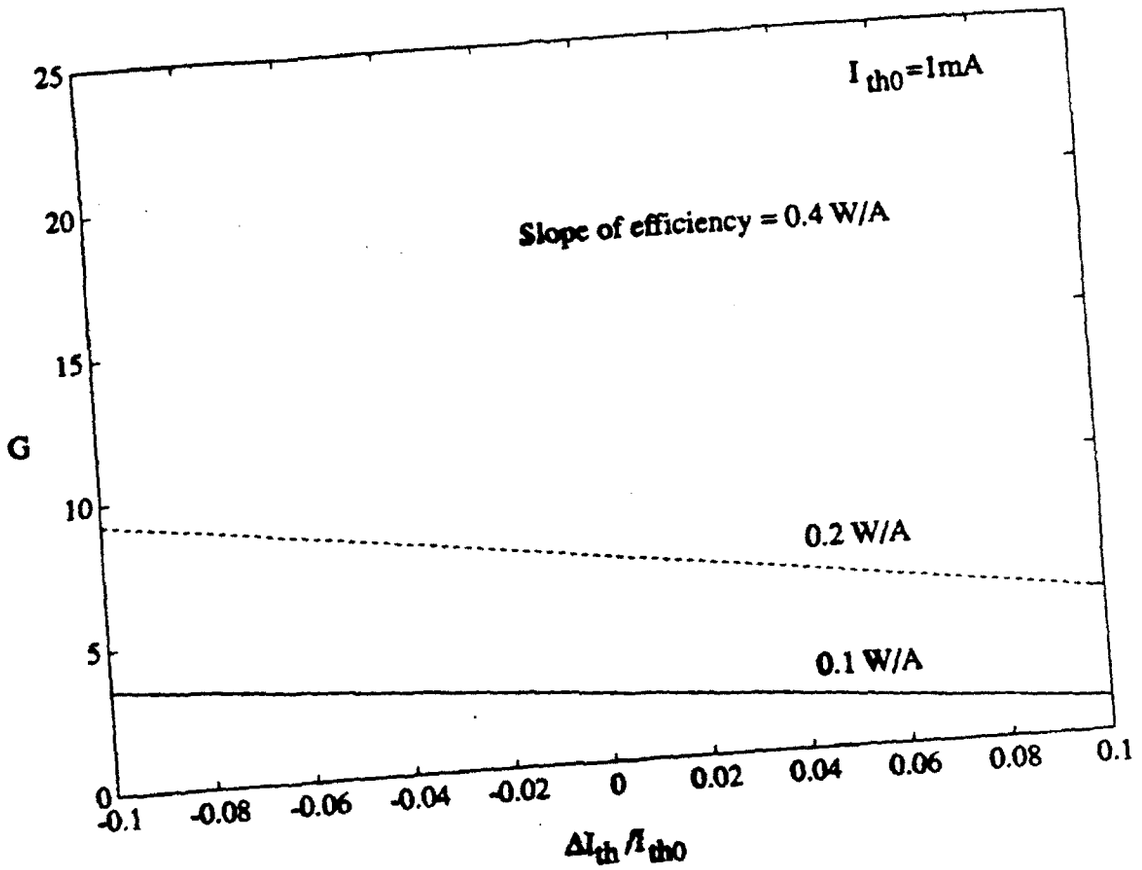

I_{th0}=1mA
Slope of efficiency = 0.4 W/A
0.2 W/A
0.1 W/A
G
25
20
15
10
5
0
-0.1
-0.08
-0.06
-0.04
-0.02
0
0.02
0.04
0.06
0.08
0.1
$\Delta I_{th}/I_{th0}$

Fig. 13

Revised

Implementations of Smart Pixels for Optoelectronic Processors and Interconnection Systems. II. SEED-based Technology and Comparison with Optoelectronic Gates

Song Yu and Stephen R. Forrest
Advanced Technology Center for
Photonics and Optoelectronic Materials (ATC/POEM)
Department of Electrical Engineering
Princeton University
Princeton, NJ 08544

Abstract

In Paper I we discussed the optoelectronic approach to the implementation of smart pixels for optical interconnection and optical computing systems. In this second paper, a similar analysis is done for SEED-based technologies. The technologies investigated include the symmetric SEED(S-SEED), asymmetric Fabry-Perot (ASFP) SEED, shallow quantum well SEED, and FET-SEED. Of these technologies, it is found that FET-SEED (whose structure is closely similar to optoelectronic logic gates) has the highest sensitivity and operates at the highest bandwidth. We then compare the advantages and limitations of the two approaches considering such system performance issues as the maximum information flux density, temperature sensitivity, and optical coupling efficiency. We conclude that the optoelectronic approach is useful in applications which require

high bandwidth ($> 1GHz$), complex logic functions, and moderate pixel density, while the SEED-based approach is more suitable to high density interconnections used at moderate bandwidths ($< 100MHz$). Furthermore, the maximum information flux density of 2D optoelectronic and FET-SEED logic gates is approximately $200GHz/cm^2$, which is from one to two orders of magnitude larger than for other SEED-based array technologies.

Implementations of Smart Pixels for Optoelectronic Processors and Interconnection Systems. II. SEED-based Technology and Comparison with Optoelectronic Gates

Song Yu and Stephen R. Forrest
Advanced Technology Center for
Photonics and Optoelectronic Materials (ATC/POEM)
Department of Electrical Engineering
Princeton University
Princeton, NJ 08544

1 Introduction

As discussed in Paper I, the implementation of smart pixels for optical interconnection and optical computing systems can be categorized into two groups. One group uses laser diodes driven by a modulated input photocurrent, and is represented by optoelectronic logic circuits which were analyzed in Paper I. The other group uses light intensity modulators and are represented by SEED-based technology [1], which will be discussed here.

The operation of self-electro-optic effect devices (SEEDs) is based on the intensity dependent nonlinear absorption change of a multiple quantum well structure due to the quantum confined Stark effect[2]. Currently SEEDs are based either on GaAs/AlGaAs or InP/InGaAs materials. In this paper we will concentrate on the GaAs/AlGaAs materials, but the discussion is also applicable to InGaAs/InP-based SEEDs. The most heavily investigated

device consists of a pair of SEEDs connected in series, known as a symmetric SEED (or S-SEED)[3]. The S-SEED has the advantages of having differential optical inputs and outputs which are relatively immune from device structural variations, and does not require critical biasing [3]. Another advantage of the S-SEED arises from its simple device structure. For the optoelectronic NOR gate that we have discussed in Paper I, the integration of a laser diode with two p-i-n photodiodes and two HBTs is an extremely complex task as compared to the integration of S-SEEDs which consist of only two identical p-i-n diodes. For this reason, S-SEED-based large scale systems have already been implemented [4-6], whereas the similar systems have yet to be demonstrated using optoelectronic integrated circuits (OEIC) logic gates. Although 4x4, 32x16, 64x32 [4-6] S-SEED based interconnection array schemes have been implemented, their performance still falls short of what has been achieved using all-electronic switching fabrics. One purpose of this analysis will be to determine the fundamental limitations confronting SEED-based technologies.

In addition to the S-SEED, there are other similar device structures with improved characteristics. Among these are the extremely shallow quantum well S-SEED [7] which can reduce the so-called exciton saturation effect[8], and the asymmetric Fabry-Perot (ASFP) SEED[9] which has a high on-off contrast ratio. The most recent research on SEED-based smart pixels has included combining transistors with SEEDs, such as the FET-SEED[10], and the logic SEED (L-SEED)[11]. These latter devices represent attempts to improve the switching speed and/or functionality of the S-SEED while achieving compatibility with existing integrated electronics. The characteristics of all of these structures will be discussed below.

The paper is organized as follows: in Section 2, we explain how S-SEED NOR gates

function. In Section 3, we analyze the noise sources governing the operation of the SEED-based logic gate. In Section 4, gain, bandwidth, and switching energy issues are discussed, while Section 5 deals with power dissipation and pixel packing density. Temperature sensitivity of SEED-based logic gates is discussed in Section 6. In Section 7, we compare the optoelectronic approach with SEED-based approaches from an interconnection/processing perspective. Finally, in Section 8, we present conclusions for the overall smart pixel study.

2 S-SEED NOR Gates

Typical optical responsivity and transmission data (at low light intensity) for a SEED as a function of reverse bias voltage are shown in Fig. 1 [12]. When the bias is zero, the exciton absorption is at a maximum. Thus, the responsivity, defined as the photocurrent generated per unit optical input power, is also at a maximum (Fig. 1a) while the transmission of the SEED is at a minimum (Fig. 1b). As the reverse bias increases, the exciton absorption peak shifts to shorter wavelength such that the responsivity decreases and the optical transmission increases. Thus, the light intensity is modulated by changing the electric field across the SEED.

A two-stage cascaded S-SEED is shown in Fig. 2 [12]. The two diodes of a S-SEED are electrically connected in series and placed under reverse bias. The state of the S-SEED is set by two input beams of different power such that most of the supply voltage drops across one diode (which has the smaller illumination intensity) while the voltage across the second device remains small. Consequently, the diode which drops only a small voltage absorbs more light than the highly biased device such that the optical outputs of the two diodes are complementary. For example, the logical "0" of the S-SEED gate is defined as the state

where the output of the upper diode is less than the output of the lower diode, while the logical "1" is the contrary state. If the S-SEED is preset to "0", it will not change its state to "1" unless both of the two input S-SEEDs are "0", and hence the S-SEED functions as a NOR gate. After the logic state of the S-SEED has been set, two reading (or clock) beams of equal power (P_{clk}) are incident on the two SEEDs, and the resulting outputs serve as the inputs to the next S-SEED stage in a free-space, cascaded 2D interconnect configuration [12]. Thus, S-SEED logic gates are differential: i.e. it is the **difference** between the two input beams that switches the the state of the logic gate. The "0" inputs to a S-SEED are the outputs from the S-SEEDs of the previous stage, which are given by [12]:

$$P_{in1} = \eta_c T(0) P_{clk}/F, \tag{1}$$

and

$$P_{in2} = \eta_c T(V_0) P_{clk}/F, \tag{2}$$

where V_0 is the supply voltage, $T(0)$ ("off") and $T(V_0)$ ("on") are the optical transmission coefficients of the upper and lower diodes, respectively, $F \geq 1$ is the fanout defined as the maximum number of pixels in an array that can be switched by the output from a single pixel in the preceding stage, and η_c is the optical coupling efficiency between the two cascaded stages of S-SEED arrays. Applying Kirchoff's current law to the S-SEED, the transient equation for the voltage at the node between the two diodes, $V_2(t)$, is [12]:

$$C_{tot}\frac{dV_2(t)}{dt} = S(V_0 - V_2)P_{in1} - S(V_2)P_{in2}, \tag{3}$$

where $S(V_0 - V_2)$ and $S(V_2)$ are the voltage-dependent responsivities, and C_{tot} is the total capacitance of the two diodes. The switching time is obtained by integrating Eq.(3) over the

voltage V_2 from $V_2 = V_0$ ("0") to $V_2 = 0$ ("1") [12]:

$$\Delta t = \int_{V_0}^{0} \frac{C_{tot}}{S(V_0 - V_2)P_{in1} - S(V_2)P_{in2}} dV_2, \tag{4}$$

Substituting P_{in1} and P_{in2} into the above equation from Eq.(1) and Eq. (2), we obtain:

$$\Delta t = \frac{C_{tot}F}{T(0)\eta_c P_{clk}} \int_0^{V_0} \frac{1}{S(V_2)CR - S(V_0 - V_2)} dV_2, \tag{5}$$

where $CR = T(V_0)/T(0)$ is the contrast ratio between the "on" and "off" diodes. Further discussion of the switching time and its effect on system performance is presented in Sec. 4.

3 Noise Analysis

In a S-SEED logic gate, the two MQW p-i-n diodes function as both light modulators and photodetectors. Ideally, the switching process occurs whenever the ratio of the power of the two input beams becomes large enough to make the photocurrent in one diode exceed that in the other. Practically, there is a "decision level" determined by the difference of the two input powers which change the state of the S-SEED logic gate. Using Eq. (3) and (4) along with the data in Figure 1, and assuming that the voltage supply is $V_0 = 20V$ and the transmission coefficients are $T(0) = 0.135$ and $T(V_0) = 0.60$, we can calculate the switching transient of a S-SEED. The changes of the transmission coefficients for the two diodes of the S-SEED during switching at different input power levels are shown in Fig. 3. Note that at the point where the transmission coefficients (or equivalently, the photocurrents) of the two diodes are equal, the state of the S-SEED is changed[13]. The photocurrent corresponding to this point is then defined as the decision level, D. If the bit rate (B) -allowed time frame, $2\Delta t = 1/B \simeq 1/2\Delta f$ (where Δf is the bandwidth), is too short for a given input power, then the transmission levels of the two devices are too close to D, such that a switching error

occurs. The power levels of the two input beams affect how fast the S-SEED will switch, whereas the ratio of the two input powers (or the contrast ratio in a cascaded system), determines whether the S-SEED will switch within a given time slot. Note that the factor of two in the relationship between Δt and B results since two time slots are required to both set and then to read its state. This two-step process is sometimes referred to as "time sequential gain" [1] since the reading power (P_{clk}) can be made larger than the switching power (P_{in}) to make up for losses between stages.

Since the optical power level typically ranges from microwatts to milliwatts, we can assume that Gaussian statistics apply. Hence the probability of a switching error occurring in a given time slot, Δt, is given by [14]

$$p(E) = \frac{1}{\sqrt{2\pi}} \frac{e^{-Q^2/2}}{Q}, \tag{6}$$

where

$$Q = \frac{D - s_i}{\sigma_i}. \tag{7}$$

Here D is the photocurrent at the decision level, s_i is the photocurrent generated when the SEED is either at $T(V_0)$ or $T(0)$, and σ_i is the standard deviation of photocurrent at $T(0)$ or $T(V_0)$. For a given bit error rate to be achieved by a S-SEED logic gate, a certain value of Q is required. For example, if $p(E) = 10^{-12}$, which is desirable in many applications in optical information processing, then $Q = 7$. This implies that the difference between $T(0)$ and $T(V_0)$ must be $> 14\sigma_i$ (where at low power levels, the responsivtity is inversely proportional to the transmission coefficient).

Since the photocurrent of the SEED is due to the absorption of photons, σ_i can be

represented by the noise current generated in the device:

$$\sigma_i^2 = < i_q^2 >, \tag{8}$$

where $< i_q^2 >$ is the quantum noise associated with photon absorption and subsequent exciton recombination. Assume that the average number of photons absorbed by the SEED during time slot Δt is N_0, which is given by:

$$N_0 = (P_{in1} + P_{in2})S(V_0)\Delta t/q = \frac{(CR+1)T(0)S(V_0)P_{clk}\eta_c}{2qFB}, \tag{9}$$

where $\Delta t = 1/2B$, and P_{in1} and P_{in2} are given by Eqs. (1) and (2), respectively. Since the quantum noise is the standard deviation of the input signal, then $< i_q^2 >$ is given by:

$$< i_q^2 >= [2q\sqrt{N_0}B]^2 = [4q\sqrt{N_0}\Delta f]^2 = 2qB(CR+1)T(0)S(V_0)P_{clk}\eta_c/F, \tag{10}$$

where $\sqrt{N_0}$ is the standard deviation of N_0. Thus, $< i_q^2 >$ is simply equal to the shot noise current generated in the SEED under illumination. The minimum input power required for determining the logic state of the S-SEED at a given BER is [14]:

$$P_{min} = (\frac{CR+1}{CR-1})\frac{Q}{S(V_0)} < i_q^2 >^{1/2} . \tag{11}$$

That is, P_{min} depends on the **output** power of the previous stage decreased by the losses between stages ($= P_{clk}T(V)\eta_c/F$). Figure 4 shows P_{min} vs B with BER $= 10^{-12}$, for a typical S-SEED, where CR is between 2 and 4 and the transmission coefficient of the "off" diode is $T(0) = 0.15$. The shaded area indicates the bit rate cutoff region in which the required BER can not be achieved. We can see that for low P_{clk}, (corresponding to a low P_{min}), the cutoff of B (B_{co}) is also low. To increase B_{co}, high P_{clk} is required, which also leads to an increase of P_{min}. Thus, noise performance must be traded with bit rate in a particular system implementation. This result shows that the noise-limited performance of

S-SEED logic gates are poorer than that of optoelectronic logic gates (see Part I) due to the presence of large input power required for the operation of S-SEED logic gates. Note that since the output of one stage (P_{clk}) is the input which must be detected at the second stage of cascaded arrays, we can define the ratio, P_{in}/P_{min}, as the logic gate detection margin. From Fig. 4, we see that for a S-SEED operating at $100Mb/s$, the minimum input power is $P_{in} = P_{clk}T(0) = 500\mu W \times 0.15 = 75\mu W$ and $P_{min} \simeq 2\mu W$. Hence, the detection margin, P_{in}/P_{min}, is about $15dB$ which is comparable to that of optoelectronic NOR gates operating at $1Gb/s$. This suggests that the optoelectronic logic gates have improved noise performance at high bit rates, although in neither case is the detection margin unacceptably small (i.e. $< 10dB$).

To improve the noise performance of the S-SEED, $T(0)$ should be minimized for a given contrast ratio. The role of contrast ratio is not obvious since it can be increased either by increasing the transmission coefficient of the "on" diode, or by decreasing that of the "off" diode. Since the ASFP S-SEED has a $T(0)$ that is very small and the photocurrent is mostly due to $P_{clk}T(V_0)$ while the input power of the logical "1" remains high due to the finite $T(V_0)$, we can expect that the ASFP S-SEED has somewhat improved noise performance.

For the FET SEED, the noise performance analysis is similar to that used for the optoelectronic NOR gate employing a p-i-n photodiode and HBT circuit. Therefore, the noise current of FET-SEED is given by[14]:

$$< i_{FS}^2 >= [\frac{4kT}{R}(1 + \frac{\Gamma}{g_m R}) + 2qI_g]I_2 B + 4kT\Gamma\frac{(2\pi C_t)^2}{g_m} I_3 B^3, \qquad (12)$$

where R is the bias resistance for the SEED that functions as a photodetector, I_g is the gate leakage current, Γ is a numerical factor which is about 1.1 for GaAs FETs, and C_t is the sum of the SEED, stray, gate-source and gate-drain capacitances. At the input of FET-SEED

logic gates, the SEED functions as a p-i-n photodiode. We expect the noise performance of FET-SEED therefore, to be similar to that of optoelectronic logic gates. Figure 5 compares the minimum time-average detectable input power P_{min} of the S-SEED, ASFP S-SEED, and FET-SEED vs B using $P_{clk} = 500\mu W$ for a BER of 10^{-12} along with the parameters listed in Table 1. We see that P_{min} of the FET-SEED is lowest among the three different device structures. The cutoff of bit rates of the S-SEED and the ASFP SEED following the treatment in Fig. 4 are also shown in the plot.

In summary, for the S-SEED logic gate to operate at high switching speeds, a high reading beam power (P_{clk}) is required (Eq. (5)), which increases P_{min} proportionally according to Fig. 4. As in the case of optoelectronic gates, low input power results in high sensitivity, but only at low bit rates. Device structures incorporating transistors such as the FET-SEED are preferred to improve the noise performance of SEED-based logic gates.

4 Bandwidth and Switching Energy

The switching speed of a S-SEED logic gate is set by the time it takes to charge the capacitance of the reverse biased MQW p-i-n diodes, which is given by Eq. (5). The switching time of the NOR gate is inversely proportional to the input signal power, or, as in cascaded S-SEEDs, the power of the reading beam, P_{clk}. This suggests that high optical power is required to achieve high speed switching. Since the capacitance of the SEED scales with its area, reducing the device area thereby proportionately increases the switching speed. However, small device area gives rise to optical alignment problems as well as to junction heating for high power input. Note that from Eq. (5), a high contrast ratio reduces the switching time. Thus Fabry-Perot structures such as the ASFP-SEED are favored for their high con-

trast ratio. The voltage for reverse biasing the SEEDs (V_0) should be as low as possible to minimize the switching time while it must be large enough to induce a sufficiently large CR.

To evaluate switching speed, detailed responsivity data of the SEED as a function of input power and operating wavelength are required. For our calculations, we use experimental data from references [7], [12], and [15] for extremely shallow quantum well S-SEEDs, conventional S-SEEDs, and ASFP S-SEEDs, respectively. Figure 6 shows the bit rate vs P_{clk} for various device structures. All the parameters used can be found in Table 1 which lists recent experimental results for the S-SEED, ASFP-SEED, and FET-SEED. In all cases, the device area is normalized to $5 \times 5\mu m^2$. The calculated results are one to two orders higher than the experimental results reported by Lentine, et al[12]. There are several possible explanations for the relatively poor experimental performance of SEED-based devices. For example, at high input powers necessary to drive the SEED at high bandwidth, the exciton saturation effect decreases the responsivity of the SEED[8]. In this case, the switching speed is no longer linearly proportional to the input power. Figure 7 shows the observed degradation of contrast ratio as input power increases. Assuming that the degradation is linear, the slope is $\sim 3.5/mW$ for conventional SEEDs and $\sim 2/mW$ for shallow QW SEEDs. The effect of this power dependent contrast ratio on the bit rate is shown by the dashed curves in Figure 6. It is apparent that the bit rate decreases by factor of 2 to 4 at high powers when the exciton saturation effect is included.

The exciton saturation effect not only degrades the contrast ratio, but also results in a decrease in responsivity [8]. A decrease of responsivity leads to a reduction in photocurrent, which, in turn results in a longer capacitance charging time. In fact, recent experimental results [12] show a bit rate of $12.5Mb/s$ for $5 \times 5\mu m^2$ S-SEED at $P_{clk} = 500\mu W$, which is

more than one order of magnitude lower than the calculated result in Fig. 6. Therefore, we may reasonably expect the maximum bit rate of S-SEED logic gates will be less than our calculated (ideal) value by a factor of $5 - 10$, and hence SEED-based arrays will be limited to $B < 100Mb/s$. Note, however, that the capacitance effects are not sufficient to explain the difference between calculation and experiment. SEED heating is an additional factor which contributes, as will be discussed in Sec. 6.

For the case of the FET-SEED or other combinations of transistors and SEEDs, the switching time is determined by the RC time constant of the input stage where the SEED performs as a photodiode. Thus the bit rate or bandwidth of FET-SEEDs can be evaluated in a fashion similar to that of optoelectronic logic gates as discussed in Paper I.

In principle, the minimum switching energy of a S-SEED logic gate is determined by the optical energy needed to generate the charge for switching the logic state of the device[1]:

$$E_{sw} = \epsilon \frac{h\nu}{q} A \mathcal{E}. \tag{13}$$

Here ϵ is the dielectric constant of the material, A the device area, and $\mathcal{E}$ the electric field. Alternatively, the switching energy can be given by the product of input power and switching time:

$$E_{sw} = (P_{in1} + P_{in2})\Delta t/2, \tag{14}$$

where P_{in1}, P_{in2}, and Δt are given by Eqs. (1), (2), and (5) respectively. Fig. 8 shows E_{sw} is plotted versus bit rate. Using the parameters given in Table 1, $V_0 = 19V$ and $A = 5 \times 10 \mu m^2$, Eq.(14) gives a switching energy of $200fJ$. This is compared with the experimental result, in which the switching energy of the same S-SEED is about $2.5pJ$[12]. The order of discrepency is consistent with the discrepency between the calculated and the experimental values of the

bit rate, and hence is attributed to exciton saturation and parasitic capcitance effects which are not included in these simple expressions.

5 Power Dissipation and Pixel Packing Density

In a S-SEED logic gate, power dissipation arises from the photocurrent flowing in the two series p-i-n diodes and the external bias circuit. Assume that a S-SEED is being switched from the "0" state to the "1" state. Then, the reverse-biased voltage drop across the upper diode will increase from approximately 0 to V_0, while the lower diode voltage decreases by the same amount. Thus the power dissipated during switching is given by

$$P_s = \int_0^{V_0} I_{ph1} dV_1 + \int_{V_0}^{0} I_{ph2} dV_2. \tag{15}$$

where the photocurrents are changing during switching, and are given by the product of input signal power and the responsivity. Since the responsivities of the two diodes are assumed to be identical, P_s can be written as

$$P_s = (P_{in1} + P_{in2}) \int_0^{V_0} S(V) dV. \tag{16}$$

During the reading of the state of the S-SEED, the power dissipation is given by the constant photocurrent generated by the clock beam:

$$P_r = I_{ph}(V_1 + V_2) = I_{ph} V_0 = P_{clk} S(V_0) V_0. \tag{17}$$

Therefore the average power dissipation for the S-SEED is given by

$$P_d = \frac{1}{2}(P_s + P_r) = \frac{1}{2}[(P_{in1} + P_{in2}) \int_0^{V_0} S(V)\, dV + P_{clk} S(V_0) V_0]. \tag{18}$$

In a cascaded circuit, the input signals are determined from the output powers of the previous stage as expressed in Eq.(1) and Eq. (2). For a S-SEED operated under low voltage ($\sim 5V$),

the power dissipation can be as low as $100\mu W$ for a $5 \times 5\mu m^2$ device operated at $100Mb/s$. Assuming that the maximum power that can be removed from a pixel array using passive cooling is $\leq 1W/cm^2$, the pixel packing density vs bit rate for various device structures is shown in Fig. 9. The pixel packing density of the ASFP S-SEED and the shallow quantum QW S-SEED are predicted to be $10^4/cm^2$ at a bit rate of $100Mb/s$. At higher bit rates, higher power input is necessary, and additional input power is consumed to overcome the exciton saturation effect. In this case, the pixel packing density drops more rapidly, as is also shown in Fig. 9. Thus we may expect the power dissipation of S-SEEDs to approach that of optoelectronic logic gates at the highest attainable bandwidths ($\geq 100Mb/s$).

Other limiting factors to the pixel packing density include geometrical and optical restrictions. For SEEDs with an area of $5\mu m \times 5\mu m$, a S-SEED logic gate would have a minimum linear dimension of approximately $20\mu m$ assuming the space between devices is on the order of the device size. This results in a maximum pixel density of $2.5 \times 10^5 cm^{-2}$. Thus, at low bit rates, this geometrical restriction should limit the pixel packing density. The complexity of optics required for the operation of the S-SEED may also impose a limit on the maximum pixel packing density (see below).

6 Temperature Sensitivity

The thermal sensitivity of S-SEEDs arises from the nature of the narrow, exciton absorption peak. In order to obtain a high contrast ratio, a narrow zero-biased exciton peak in the absorption spectrum is desirable. This, in turn, requires an input with its wavelength precisely tuned to the absorption peak that has a width of only a few nanometers. As temperature fluctuates, the exciton absorption peak deviates from its original wavelength due to

the temperature dependence of the bandgap energy. For GaAs, the temperature dependence of bandgap energy $\mathcal{E}_g$ is given empirically by[16]

$$\mathcal{E}_g(T) = 1.522 - \frac{5.8 \times 10^{-4} T^2}{T + 300} \tag{19}$$

where $\mathcal{E}_g$ is in eV and the temperature, T, is in Kelvin, with a similar equation for InP-based materials. This relation gives $d\mathcal{E}_g/dT = 0.4meV/K$ or $d\lambda/dT = 0.25nm/K$ for $\lambda = 850nm$ at room temperature. This temperature sensitivity is shown by the contrast ratio vs temperature curve in Fig. 10, which is calculated using data from references [7] and [9]. We see that the contrast ratio of a ASFP SEED decreases by a factor of 10 as the temperature changes by $\pm 5K$. Thus, if the system temperature is changed, the contrast ratio of the ASFP SEED will drastically decrease. With constant input power, the switching time of the S-SEEDs will also be substantially increased (c.f. Eq. (5)), which in turn will increase the bit error rate. To avoid this effect, it is necessary to stabilize the temperature of ASFP SEEDs to within $\sim 1K$. On the other hand, S-SEEDs are less temperature sensitive due to their smaller contrast ratio.

Since the high speed operation of S-SEEDs demands that high incident optical power be focussed on a rather small device area, the high intensity of the light will inevitably result in device heating which will, in turn, lead to variations of bandgap[17]. The steady-state temperature rise of the SEED relative to the ambient is proportional to the heat generation rate in the SEED:

$$\Delta T = R_T P_d/2, \tag{20}$$

where $P_d/2$ is the total power dissipated by a single SEED as given by Eq. (18), and R_T is

the thermal resistance which is given by [18]:

$$R_T = \frac{1}{A}(\frac{d}{\kappa}) + \frac{1}{4\pi\kappa}. \tag{21}$$

Here, A is the SEED area, d is the thickness of the SEED mesa, and κ is the thermal conductivity of the material. The first term of Eq. (21) is due to the thermal resistance of the mesa, whereas the last term is the thermal resistance of the semi-infinite substrate. The results of Eq. (20) are shown by Fig. 11 for $d = 1\mu m$, $\kappa(GaAs) = 0.44W/cmK$, and $A = 25\mu m^2$. We see that the temperature rise of the SEED during a reading pulse can be several degrees, which will shift the exciton absorption peak and degrade the contrast ratio of the SEED. That is, a 50% decrease of CR occurs if the device temperature increases by only 2 to 3 K.

While Eq. (20) is for the steady-state case, it is also important under high bandwidth (and therefore high power) conditions to examine the SEED thermal transient response. In this case, the rate of temperature change, dT/dt, is proportional to P_d/mC_v, where m is the mass of the SEED, and C_v is the specific heat of the material. Assuming that at $t = 0$ light input switches off in a step-wise manner, the thermal transient equation for $t > 0$ is then given by:

$$\frac{A}{d}\kappa T + mC_v\frac{dT}{dt} = 0. \tag{22}$$

This results in a characteristic thermal time constant of:

$$\tau_T = \frac{mdC_v}{A\kappa}. \tag{23}$$

Here, $\tau_T = 10^{-6}sec$ for GaAs, where $C_v = 0.32J/g - K$, $m = \delta dA$, with the density $\delta = 5.32g/cm^3$ for GaAs. This implies that since the SEED switching time is shorter than

τ_T, the heat generated during a pulse will not be completely removed at high bandwidths. Thus, the device temperature will increase and the contrast ratio will degrade. Another issue is the effect of bit pattern on the thermal dissipation of SEEDs. Due to the long τ_T of the SEED, long pulses at the input of the SEED will cause the accumulation of heat on the device, and will further degrade its performance.

7 Comparison of Smart Pixel Technologies

7.1 Information Flux

The major potential advantages that optical interconnections have over their electrical counterparts are the high bandwidth and parallelism of channels offered by optics. Although various applications emphasize different device characteristics, the overall performance of a system must be evaluated by including both of these factors. Thus the maximum amount of information flowing through the interconnection is the parameter which defines the total capacity of the system. We define the "information flux" of an interconnection system as the product of the bandwidth of each channel and the maximum allowed channel packing density, viz:

$$\mathcal{F} = \Delta f \, \rho, \tag{24}$$

where Δf is the bandwidth, and ρ is the pixel packing density. Based on our calculations and discussion in previous sections and in Paper I, $\mathcal{F}$ is plotted versus bandwidth and pixel packing density in Figs. 12 and 13, respectively, assuming that the S-SEED device area is $5 \times 5 \mu m^2$ and the detector area in OEIC and FET-SEED gates is $10 \times 10 \mu m^2$. As shown in Fig. 12, cascode OEIC circuits offer the highest bandwidth of all the technologies. Such bandwidths are required in some high performance systems, although the information flux

density is not the highest attainable due to the additional power dissipation of cascode circuit. For logic gates operated at low power, geometrical restrictions will physically limit the maximum pixel packing density. This is shown in Fig. 12 by the linear decrease in $\mathcal{F}$ at low bandwidth. For example, an optoelectronic NOR gate consisting of a laser diode output, two photodiodes and a HBT circuit would have an approximate minimum linear dimension of $\sim 140\mu m$ assuming the laser is a surface emitter with $20\mu m$ total diameter, the p-i-n diode diameter is $20\mu m$, and the HBTs are $10\mu m$ on a side. Then the maximum pixel density is geometrically limited to $5000cm^{-2}$, which gives the cutoff line for the optoelectronic curve in Fig. 13. Similarly, S-SEED logic gates with a feature size of $5\mu m$ on $20\mu m$ centers would have a cutoff at $\sim 10^5 cm^{-2}$.

According to our analysis, the maximum information flux that can be achieved by the optoelectronic approach is $\sim 200GHz/cm^2$, where $1W/cm^2$ is taken as the maximum chip power dissipation allowed assuming passive cooling. With active cooling, power dissipations of $10 - 100Wcm^{-2}$ can be achieved, in which case the maximum value for $\mathcal{F}$ can be $2 - 20THz/cm^2$. It is useful to compare this value of $\mathcal{F}$ to that which can be achieved using competitive electronic (Si VLSI) technology. Although a direct comparison is difficult, we can consider the following: with Si VLSI, transistor densities as high as 10^6/chip are typical. However, the I/O density is given by the empirical relationship known as Rent's Rule [19], where:

$$I/O = k(N_g)^{1/c}, \tag{25}$$

where k and c are constants, and N_g is the number of gates. For $N_g = 10^4$ for $1cm^2$ chip, $k = 0.5$, and $c = 1.8$ typical of Si VLSI, we obtain I/O$\simeq 10^2 cm^{-2}$. This is compared with the optical approach, where I/O$= N_g$ can be obtained in some systems. Hence, given that Si

VLSI bandwidths approach $200MHz$, we obtain an effective flux density of $\mathcal{F}= 20GHz/cm^2$, which is one order of magnitude less than the OEIC result. Alternatively, if we do not constrain our system limitations to the I/O density but rather to the number of gates, then we obtain $\mathcal{F}= 1THz/cm^2$. In this comparison, the Si VLSI information flux density is 5 to 10 times larger than that of optoelectronic integrated circuits. However, conventional VLSI circuits can not be operated at high bandwidth $> 1GHz$ due to the crosstalk between the metal wires used in integrated circuits. Optoelectronic circuits have greatly reduced crosstalk between pixels at high bandwidth, particularly if optical powering of optoelectronics is used, as has been shown in previous work [20]. Another advantage of using optics is that by using photons as the information carrier, the requirement of impedance matching, which is a critical limitation in conventional VLSI, can be lifted since photons are noninteractive.

It is clear that the optoelectronic and FET-SEED approaches have a higher $\mathcal{F}$ than SEED-based technologies in the high bandwidth range although it offers only a medium-grained pixel packing density of $\leq 200/cm^2$. Since the the fundamental advantages of bringing optics into large-scale switching and information processing system applications relies on the need for both high bandwidth and parallelism, we have to make trade-offs between these factors for optimal use in a specific application. For optical computing and information processing which demand very high bandwidth, the optoelectronic approach provides a clear advantage. Indeed, from Fig. 12 and Fig. 13 we see that optoelectronic gates provide an information flux of one to two orders of magnitude higher than SEEDs at channel bandwidths exceeding $1GHz$. On the other hand, due to the relaxed geometrical restrictions of the SEEDs, their flux density is higher at $\Delta f \leq 10MHz$.

S-SEED logic gates suffer from the large voltage needed to sustain a usable contrast

ratio, which leads to long switching time and high power dissipation. However, recently demonstrated SEEDs require a supply voltage of only $\sim 5V$, which considerably decreases the switching time and power dissipation [21]. Nevertheless, the exciton saturation effect still remains the fundamental limit to the performance of SEED-based logic gates. Although extremely shallow quantum well SEEDs have been employed to reduce the exciton saturation effect, this device also causes the exciton bound state to be easily ionized at low field. This causes the exciton absorption edge to broaden, thus limiting the contrast ratio.

As we have discussed above, a large contrast ratio is important to maintain low noise operation. A S-SEED with an ASFP structure usually can achieve high contrast ratio, but also leads to high sensitivity to wavelength and temperature. Indeed, the nature of exciton absorption leads to an inherent wavelength and temperature sensitivity of all SEED-based devices which is absent in optoelectronic logic gates. The narrow Fabry-Perot resonance peak of the ASFP SEED makes the device even more sensitive, as we demonstrated above. Also, when high optical input power is applied to the photodetector, local substrate heating will occur. For the optoelectronic case, the effect is not serious because (1) the logic gate has amplification and thus it does not require high power optical input; (2) the p-i-n photodetector can have a large area to reduce the local input power density without adversely affecting bandwidth; and (3) the wide spectral bandwidth of the photodetection process is largely insensitive to the temperature change. As opposed to optoelectronic logic gates, the SEED-based logic gates are (1) very sensitive to temperature changes due to the narrow exciton absorption peak ($d\lambda/dT = 0.25nm/K$); (2) the bandwidth is proportional to the input power (except for FET-SEEDs), which is also degraded by the exciton saturation effect; and (3) the area of the SEED strongly affects bandwidth.

7.2 Optics and Coupling Efficiency

We now consider the constraints placed on the optics between neighboring stages of an optical interconnection implemented using either optoelectronic or SEED technologies. Assuming that refractive microlens arrays are used to focus the input beams onto the photodetectors [22], the major deviation of light from the targeted photodetectors arises from astigmatic aberrations[22]. The diameter of the photodetector should therefore be larger than the aberration in order to avoid crosstalk, and to ensure high optical coupling efficiency. For the optoelectronic logic gate, the area of the p-i-n diode can be made large without seriously affecting the bandwidth of the circuit, as seen from Fig. 8 in Paper I. For example, the bandwidth will drop from $2GHz$ to $1.5GHz$ ($\beta = 25$) as the diameter of the p-i-n photodiode increases from $5\mu m$ to $15\mu m$. In a S-SEED logic gate, increasing the device area will decrease the bandwidth proportionally. For example, if the diameter of the SEED is increased from $5\mu m$ to $15\mu m$, the capacitance will be multiplied by a factor of 9, hence resulting in a concomitant reduction in the bandwidth. Furthermore, for the optoelectronic logic gates, only two input and one output beams are required, while FET-SEEDs require three and S-SEEDs require four I/O beams. In high density 2D smart pixel arrays, the implementation of complicated optics is extremely demanding. Thus minimizing the number of optical beams to be focused onto each pixel should improve the yield and lower the production costs of complex 2D interconnection systems.

Another issue related to the coupling efficiency is the fanout of the logic gates. Fundamentally, the fanout is limited by the on-off contrast ratio of the logic gate. This results since $P_{in}(on)$ should always be greater than $P_{out}(off)$ in order to maintain low noise operation.

With $P_{in}(on) = \eta_c P_{out}(on)/F$, we obtain the following condition:

$$CR = P_{out}(on)/P_{out}(off) > F/\eta_c. \tag{26}$$

Thus, CR imposes a limit on the maximum value of F. For optoelectronic logic gates, CR can be as high as 10 to 1000, thus allowing for a large fanout between stages. For simple S-SEED and FET-SEED logic gates, CR usually is about 2 to 4, hence $F > 1$ is not easy to achieve if the coupling efficiency is low. This problem can be alleviated by employing ASFP SEED structures to improve the contrast ratio.

As defined in Paper I, the fanout of cascaded logic gates is $F = \eta_c G$. Hence, as the coupling efficiency between stages decreases, the gain (and therefore the power dissipation) must be increased. Note that η_c depends on the lens loss and misalignment when coupling the light into the device. In order to maintain a high η_c, the area of the SEED should be large enough to fully cover the input beam spot. For example, assuming that the spot diameter of the input beam is $1\mu m$ and is perfectly centered on a $5\mu m$-diameter SEED, if the collimating lens has a focal length of $10mm$, it takes a positional drift of only 0.02 degree for the incident light to move completely out of the area of SEED. For a $20\mu m$-diameter SEED, it takes a 0.06-degree-drift. This estimation and detailed analysis by McCormick, et al. [23] show that the alignment tolerance is extremely tight. Thus small area SEEDs still need a high-power reading beam to compensate for coupling and fanout losses. However, the maximum instantaneous P_{clk} that can be applied is limited by the exciton saturation effect [8] and the temperature sensitivity of the SEED, which is due to substrate heating at high input powers.

For large scale integration, the non-uniformity of device characteristics will seriously impair system performance. Very often, the non-uniformity can not be easily corrected dur-

ing the fabrication process. For OEIC based circuits, the non-uniformity mainly comes from the variation of threshold current of laser diodes (see Paper I). This can be compensated by increasing the current swing of laser diodes at the expense of increased power dissipation. For SEED-based logic gates, the non-uniformity usually comes from the variation of photocurrent and refelctivity, which is compensated by the individual adjustment of bias or shift of wavelength, which is difficult to realize in large arrays. For ASFP SEEDs, it is practically difficult to operate all the pixels in a large array at the same wavelength due to the complexity of the device structures which requires extreme uniformity in the device fabrication process.

8 Summary

We have studied two different approaches to using smart pixel technology for optical interconnections. One is based on laser/electronics/detector optoelectronic integrated circuits, the other is based on SEED optical modulators. The noise performance, optoelectronic gain, bandwidth, switching energy, power dissipation, pixel packing density, and temperature sensitivity of the approaches have been analyzed and compared. The information flux of an interconnection system has been defined and used as a figure of merit for comparing the two approaches. In Table 2, we list the typical performance characteristics of devices using both approaches. The main advantages offered by optoelectronic logic gates over S-SEED-based logic gates are high bandwidth ($> 1GHz$), high optoelectronic gain, and ultimately high information flux. The main advantage of S-SEEDs is that they are much easier to integrate than both optoelectronic logic gates and FET-SEEDs. Even with recently demonstrated micro-cavity lasers, the integration of optoelectronic logic gates still has numerous techni-

cal problems to overcome. Although incorporating transistors into SEED structures such as in the FET-SEED can improve the performance of SEED-based logic gates, the strong dependence of the operating wavelength on temperature still presents inherent drawbacks to SEED-based logic gates. The functionality offered by S-SEED logic gates is also limited, while optoelectronic and FET-SEED logic gates can fully combine the advantages of optics and electronics, which results in the inherent potential of developing complex functionality required by a diversity of interconnection and processing systems.

In conclusion, the optoelectronic approach has certain advantages in information flux ($\mathcal{F} \sim 200GHz/cm^2$), bandwidth ($B \geq 1GHz$), and temperature sensitivity over S-SEED-based technologies, which nevertheless offers low power dissipation and high packing density at moderate bandwidths.

Acknowledgments

The authors thank the Air Force Office of Scientific Research (A. Craig), Rome Air Development Center/Hanscom Air Force Base (J. Lorenzo), and Siemens Corporate Research for partial support of this work.

References

[1] D. A. B. Miller, "Quantum well self electro-optic effect devices," Opt. and Quantum Electron., vol. 22, pp. S61-S98, 1990.

[2] D. A. B. Miller, D. S. Chemla, T. C. Damen, A. C. Gossard, W. Wiegmann, T. H. Wood, and C. A. Burrus, "Bandedge optical modulation with GaAs/GaAlAs quantum well structures: The quantum confined Stark effect," Phys. Rev. B, vol. 32, pp. 1043-1060, 1984.

[3] A. L. Lentine, H. S. Hinton, D. A. B. Miller, J. E. Henry, J. E. Cunningham, and L. M. Chirovsky, "Symmetric self-electrooptic effect device: Optical set-reset latch, differential modulator/detector," IEEE J. Quantum Electron., vol. 25, pp. 1928-1936, 1989.

[4] M. E. Prise, N. C. Craft, M. M. Downs, R. E. LaMarche, L. A. D'Asaro, L. M. F. Chirovsky, and M. J. Murdocca, "Optical digital processor using arrays of symmetric self-electrooptic effect devices," Appl. Optics, vol. 30, pp. 2287-2295, 1991.

[5] F. B. McCormick, A. L. Lentine, R. L. Morrison, S. L. Walker, L. M. F. Chirovsky, and L. A. D'Asaro, "Parallel operation of a 32x16 symmetric self-electrooptic effect device array," IEEE Photon. Technol. Lett., vol. 3, pp. 232-234, 1991.

[6] F. B. McCormick, F. A. P. Tooley, J. M. Brubaker, A. L. Lentine, T. J. Cloonan, R. L. Morrison, S. L. Walker, and R. J. Crisci, "Parallel integration of two 64x32 symmetric selfelectro-optic effect device array," Electron. Lett. vol. 27, pp. 1869-1871, 1991.

[7] R. A. Morgan, M. T. Asom, L. M. F. Chirovsky, M. W. Focht, K. G. Glogovsky, G. D. Guth, G. J. Przybylek, L. E. Smith, and K. W. Goossen, "Low-voltage, high-

saturation, optically bistable self-electro-optic effect devices using extremely shallow quantum wells," Appl. Phys. Lett., vol. 59, pp. 1049-1051, 1991.

[8] A. M. Fox, D. A. B. Miller, G. Livescu, J. E. Cunningham, and W. Y. Jan, "Quantum well carrier sweep out: Relation to electroabsorption and exciton saturation," IEEE J. Quantum Electron., vol. 27, pp. 2281-2295, 1991.

[9] M. Whitehead, G. Parry, P. Wheatley, "Investigation of etalon effects in GaAs-AlGaAs multiple quantum well modulators," IEE Proc. vol.136, pt. J, pp. 52-58, 1989.

[10] T. K. Woodward, L. M. F. Chirovsky, A. L. Lentine, L. A. D'Asaro, E. J. Laskowski, M. Focht, G. Guth, S. S. Pei, F. Ren, G. J. Przybylek, L. E. Leibenguth, M. T. Asom, R. F. Kopf, J. M. Guo, and M. D. Feuer, "Operation of a fully integrated GaAs-AlGaAs FET-SEED: A basic optically addressed integrated circuit," IEEE Photon. Technol. Lett., vol. 4, pp. 614-617, 1992.

[11] A. L. Lentine, F. A. Tooley, S. L. Walker, F. B. McCormick, Jr., R. L. Morrison, L. M. F. Chirovsky, M. W. Focht, J. M. Freund, G. D. Guth, R. E. Leibenguth, G. J. Przybylek, L. E. Smith, L. A. D'Asaro, D. A. B. Miller, "Logic self-electrooptic effect devices: Quantum-well optoelectronic multiport logic gates, multiplexers, demultiplexers, and shift registers," IEEE J. Quantum Electron., vol. 28, pp. 1539-1553, 1992.

[12] A. L. Lentine, D. A. B. Miller, L. M. F. Chirovsky, and L. A. D'Asaro, "Optimization of absorption in symmetric self-electrooptic effect devices: A system perspective," IEEE J. Quantum Electron., vol. 27, pp. 2431-2439, 1991.

[13] The relationship between transmission and responisivity implies that when the transmission of the two SEEDs in the pair are equal, so are the photocurrents generated in each

device. Hence, the decision level corresponds to the state in which the photogenerated currents in both SEEDs are equal.

[14] R. G. Smith and S. D. Personick, "Receiver Design for Optical Fiber Communications," Chap. 4, in Semiconductor Devices for Optical Communication, ed. H. Kressel, 1982.

[15] R. J. Grindle, J. E. Midwinter, and J. S. Roberts, "High contrast, low-voltage, symmetric-selfelectro-optic effect device (S-SEED)," Electron. Lett., vol. 27, pp. 2327-2329, 1991.

[16] C. M. Wolfe, N. Holonyak, Jr., G. E. Stillman, Physical Properties of Semiconductors, Englewood Cliffs, NJ: Prentice Hall, 1989.

[17] T. Sizer II, R. E. LaMarche, and T. K. Woodward, "Point source heating effects in MQW modulators," Conference on Lasers and Eletro-optics, pp254-255, 1992.

[18] S. M. Sze, Physics of Semiconductor Devices, New York: Wiley, 2nd ed., 1981.

[19] R. A. Nordin, A. F. J. Levi, R. N. Nottenburg, J. O'Gorman, T. Tanbun-Ek, and R. A Logan, "A system perspective on digital interconnection technology," J. Lightwave Technology, vol. 10, pp. 811-827, 1992.

[20] M. Govindarajan and S. R. Forrest, "Optically powered arrays for optoelectronic interconnnection networks,", Appl. Optics, vol. 30, pp. 1335-1346, 1991.

[21] A. L. Lentine and D. A. B. Miller,"Evolution of the SEED technology: Bistable logic gates to optoelectronic smart pixels," IEEE J. Quantum Electron., vol. 29, pp. 655-669, 1993.

[22] T. Sakano, K. Noguchi, and T. Matsumoto, "Optical limits for spatial interconnection networks using 2-D optical array devices," Appl. Optics, vol. 29, pp. 1094-1100, 1990.

[23] F. B. McCormick, Jr., F. A. Tooley, S. L. Walker, J. L. Brubaker, J. M. Sasian, T. J. Cloonan, A. L. Lentine, R. L. Morrison, R. J. Crisci, S. L. Walker, S. J. Hinterlong, M. J. Herron, "Design and tolerancing comparisons for S-SEED-based free-space switching fabics," Opt. Eng. vol. 31, pp. 2697-2711.

Figure Captions

Figure 1: Photoresponsivity (a) and transmission coefficient (b) of SEED as a function of bias voltage [from Ref. 12]

Figure 2: S-SEED NOR gate in a cascaded system. The output of the preceding stage is the input of next stage. The transmission of the two SEEDs in each S-SEED are always complementary to each other. Switching the S-SEED requires four beams: two input (P_{in}) and two reading beams (P_{clk}).

Figure 3: Switching transient of S-SEED for given P_{clk}. When the transmission coefficients of the two SEEDs are equal to each other, the logical state of the S-SEED changes. The intersection is defined as Decision Level.

Figure 4: Minimum input power (P_{min}) vs bit rate required for the S-SEED to operate at BER=10^{-12}. The shaded area correponds to BER> 10^{-12}. B_{co} is the cutoff bit rate.

Figure 5: Minimum input power (P_{min}) required for various SEED-based device structures to operate at BER=10^{-12} with $P_{clk} = 500\mu W$. B_{co} is the cutoff bit rate.

Figure 6: SEED bit rate as function of reading beam (P_{clk}) for different device structures: ideal case (solid curves) and including the exciton saturation effect (dashed curves).

Figure 7: Observed degradation of contrast ratio due to exciton saturaturation. "X" data from Ref. [12]; "O" from Ref. [7]. A linear relationship between P_{clk} and CR is assumed for the straight lines fit to the data.

Figure 8: Switching energy (E_{sw}) versus bit rate of different SEED structures. At

high bit rate (high P_{clk}), the exciton saturation effect causes an increase in switching energy, as shown.

Figure 9: Pixel packing density as function of bit rate for different SEED structures assuming that the maximum thermal power that can be removed from the pixel array is $1W/cm^2$. The exciton saturation effect is shown by the drop of pixel packing density at high bit rates. Also shown is the bit rate cutoff region.

Figure 10: Contrast ratio of the S-SEED and the ASFP-SEED as a function of temperature change.

Figure 11: Temperature rise versus optical input power assuming steady state for thermal conduction.

Figure 12: Information flux density versus bandwidth for optoelectronic logic gate and SEED-based technologies. The linear decrease of $\mathcal{F}$ at low bandwidth is due to the geometrical limits on physical size of the gates. At the high bandwidth end, cascode OEIC circuits offer the highest bandwidth of all technologies.

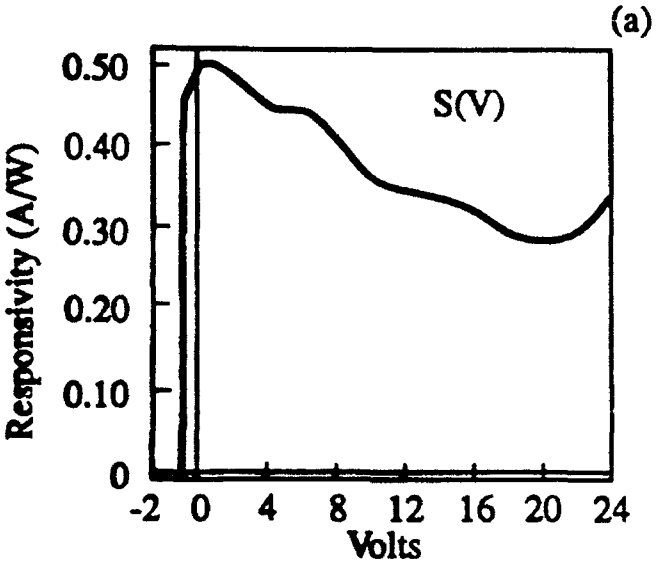
Figure 13: Information flux density versus pixel packing density for optoelectronic logic gates and SEED-based technologies. "G. L." indicates geometrical limitation.

Table 1 Parameters and Performance of SEED-based Smart Pixels

	S-SEED			FET-SEED
	original (Lentine)	shallow QW (Morgan)	ASFP (Grindle)	(Woodward)
Reference	[9]	[4]	[11]	[8]
Device Area (μm^2)	5x10	5x5	5x5	5x5
Capacitance(fF)	12	6	6	3
V_0 (V)	15	5	4.2	12
T(0) (on)	0.135	0.10	0.01	0.25
$T(V_0)$ (off)	0.55	0.37	0.22	0.15
Contrast Ratio(Power)	4.2(50μW) 1.4(500μW)	3.7(10μW) 2.0(840μW)	70(--)	2.5(1mW)
Gain	(1-2)	(1-2)	(--)	8.5-100
Switching Time (ns)	40	--	--	2.8
Switching Energy(pJ)	2.5	--	--	0.4

Table 2 Comparison of Smart Pixel Technologies

	OEIC	S-SEED	ASFP S-SEED	FET-SEED
Information Flux	200GHz/cm^2	5GHz/cm^2	50GHz/cm^2	200GHz/cm^2
Bandwidth/channel	>1GHz	100MHz	100MHz	>1GHz
Optoelectronic Gain	10-100	<10	10	10
Contrast Ratio	>100	<5	10-100	<5
Switching Energy	20fJ	200fJ	200fJ	40fJ
Power Dissipation	5mW	1mW	0.1mW	2mW
Pixel Packing Density	200/cm^2	10^3/cm^2	10^4/cm^2	500/cm^2
Wavelegth sensitivity	low	high	high	high
Temperature Sensitivity	moderate	high	high	high
Input beams required	2/pixel	4/pixel	4/pixel	3/pixel


(a)
S(V)
Responsivity (A/W)
0.50
0.40
0.30
0.20
0.10
0
-2 0 4 8 12 16 20 24
Volts

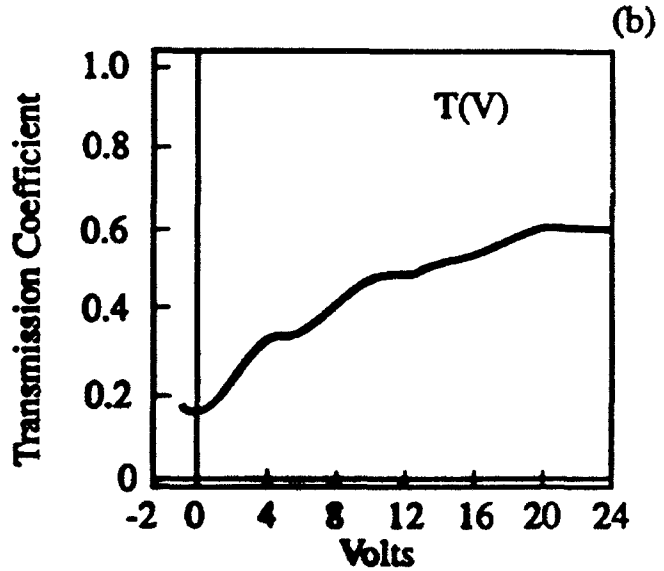

(b)
T(V)
Transmission Coefficient
1.0
0.8
0.6
0.4
0.2
0
-2 0 4 8 12 16 20 24
Volts

Fig 1

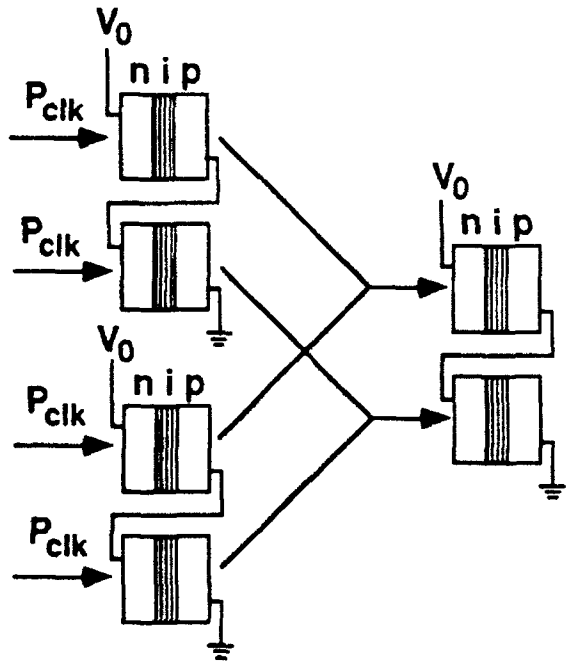


Fig. 2

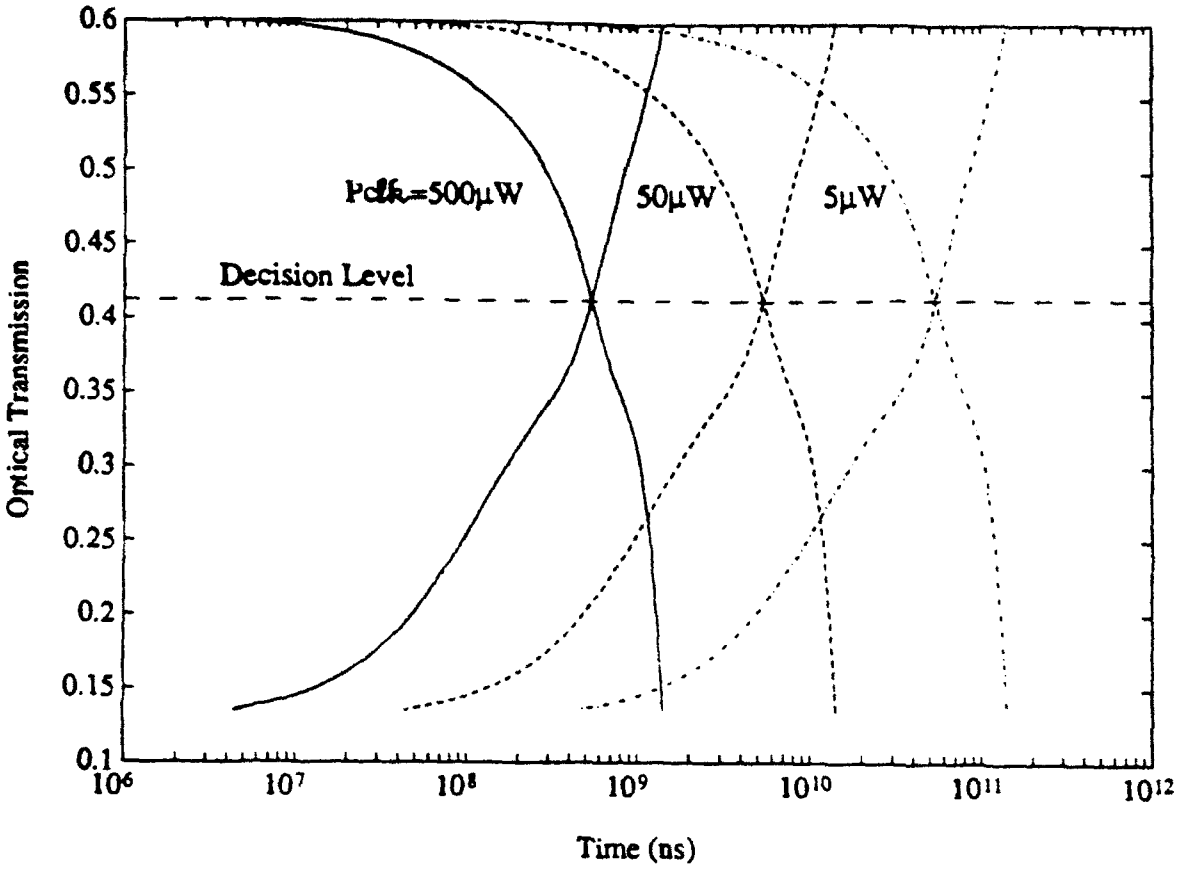

0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
Optical Transmission
Pclk=500μW
50μW
5μW
Decision Level
10^6
10^7
10^8
10^9
10^10
10^11
10^12
Time (ns)

Fig. 3

Fig. 4

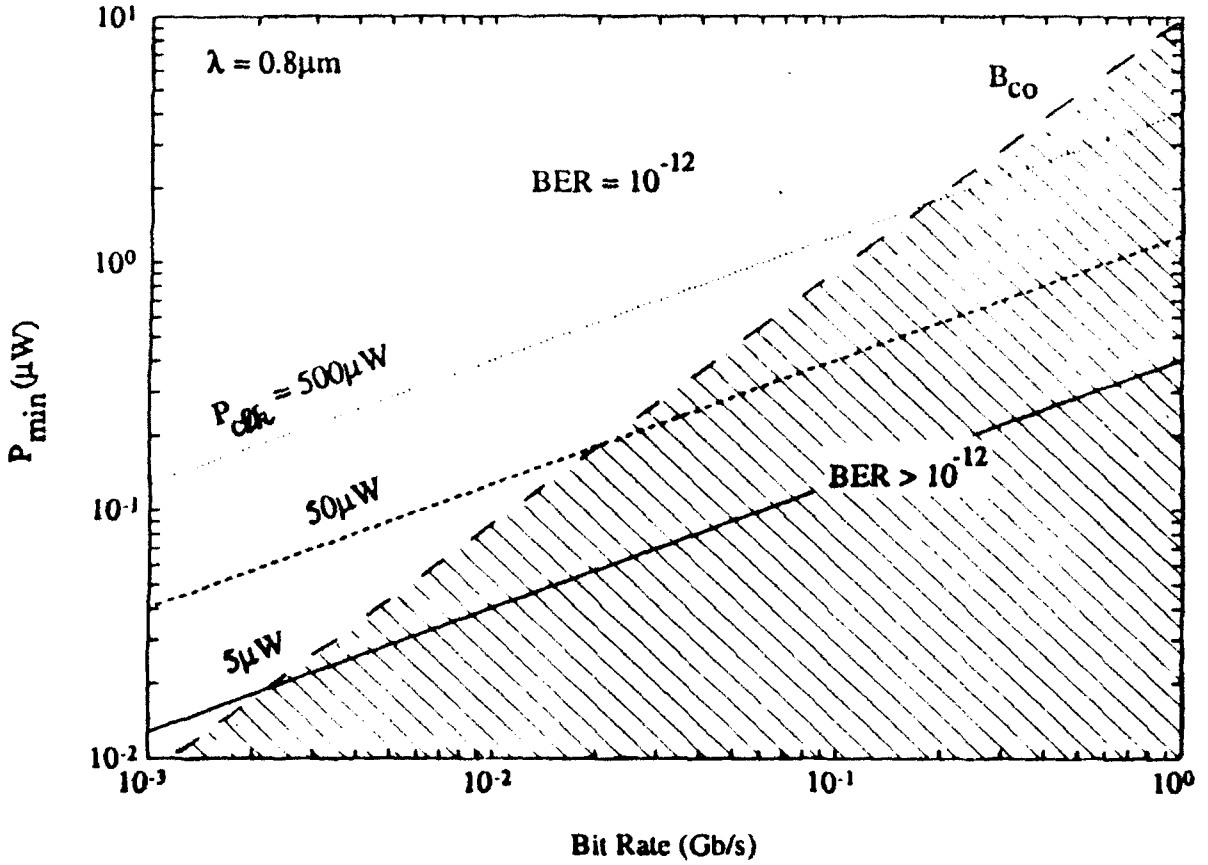
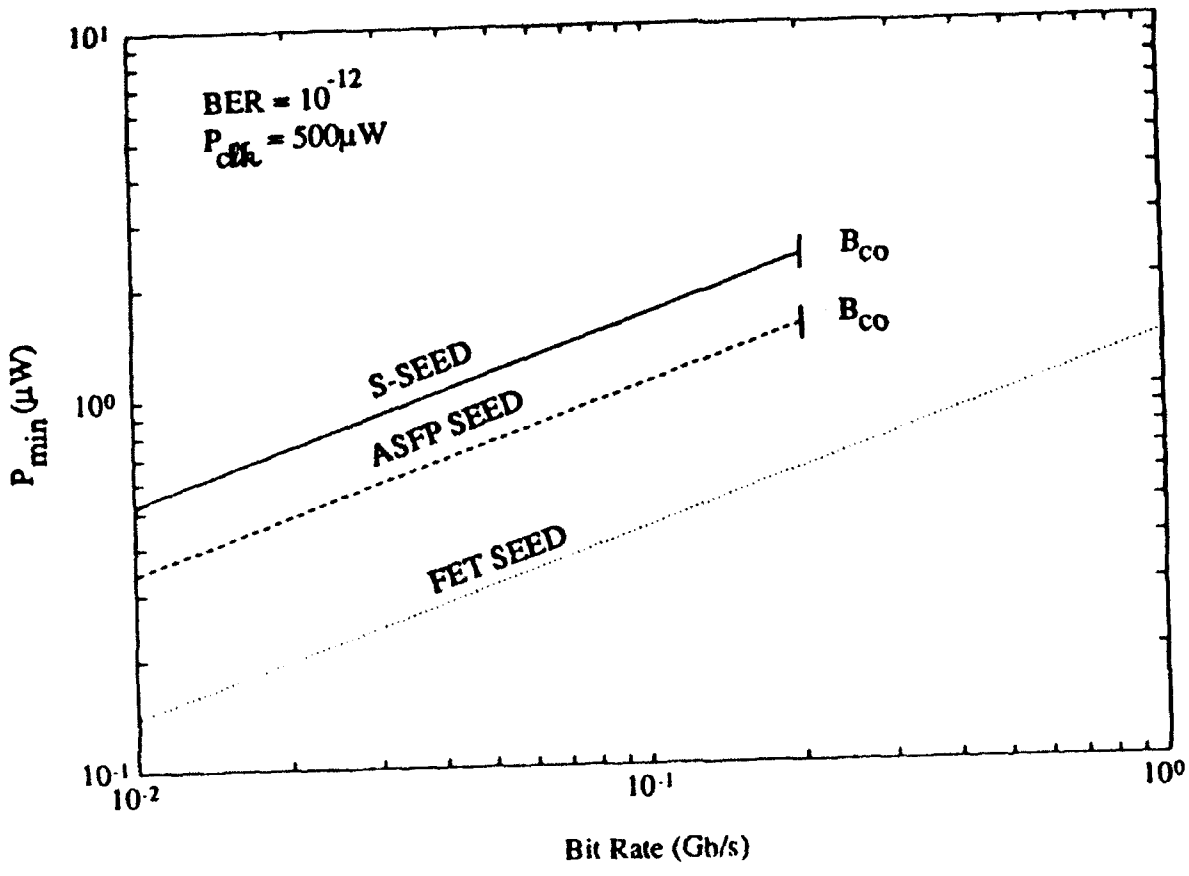

λ = 0.8μm
B_{co}
BER = 10^{-12}
P_{clk} = 500μW
50μW
5μW
BER > 10^{-12}
P_{min} (μW)
Bit Rate (Gb/s)
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-2}
10^{-1}
10^{0}

Fig. 8


BER = 10^-12
P_clk = 500μW
B_co
B_co
S-SEED
ASFP SEED
FET SEED
P_min (μW)
10^1
10^0
10^-1
10^-2
10^-1
10^0
Bit Rate (Gb/s)

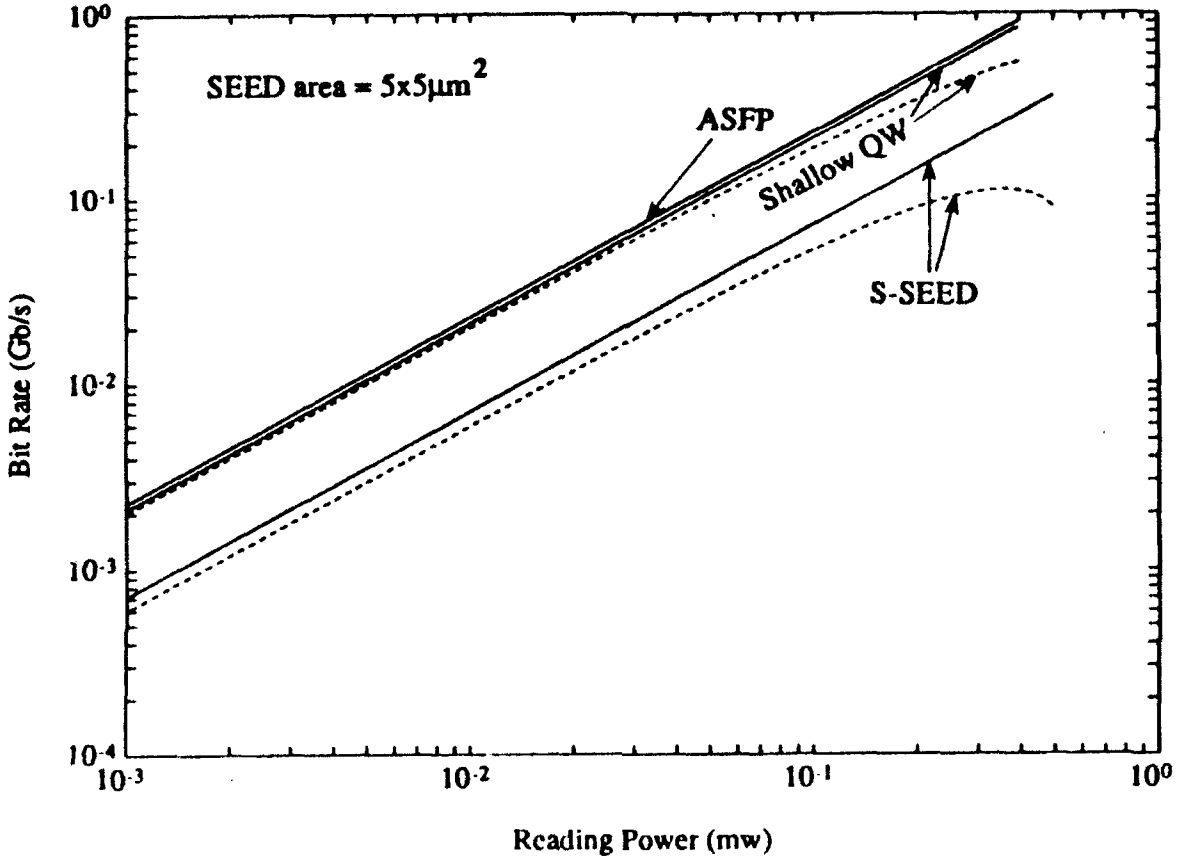

SEED area = 5x5μm²
ASFP
Shallow QW
S-SEED
Bit Rate (Gb/s)
Reading Power (mw)
10⁰
10⁻¹
10⁻²
10⁻³
10⁻⁴
10⁻³
10⁻²
10⁻¹
10⁰

Fig. 7

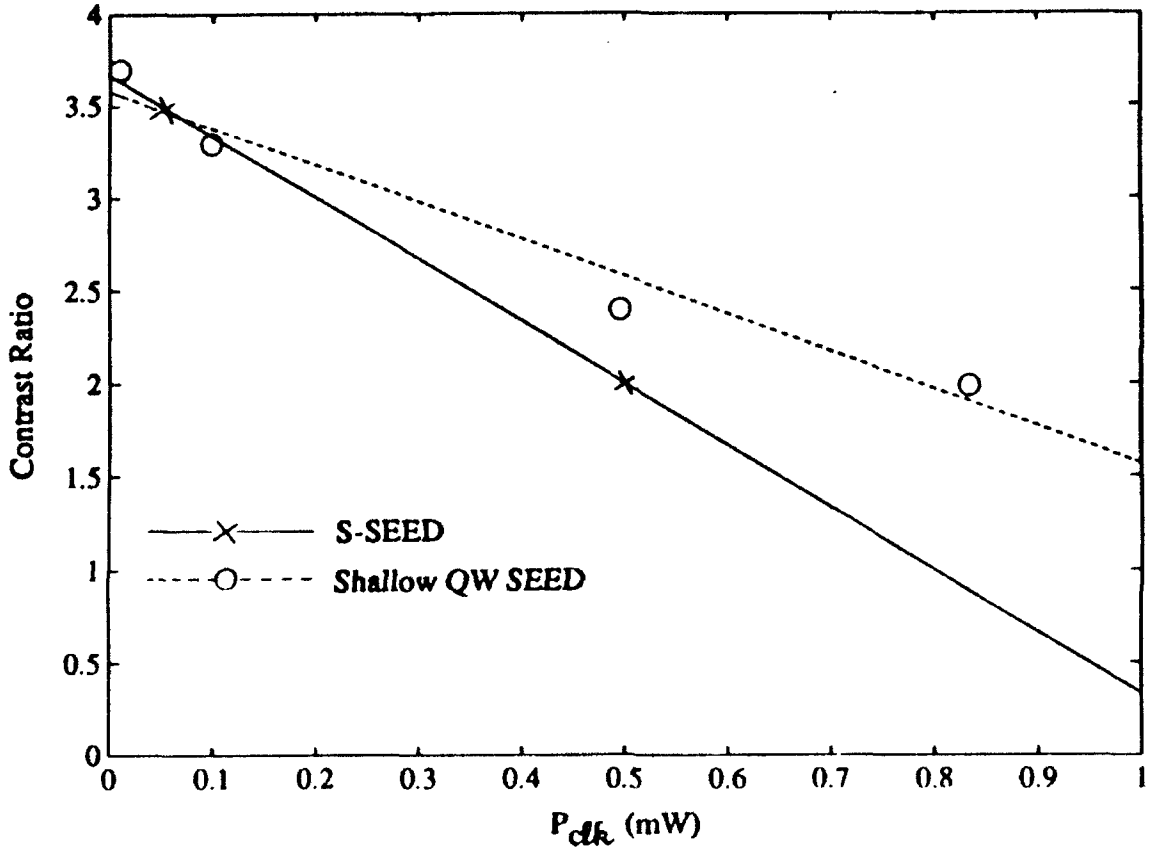
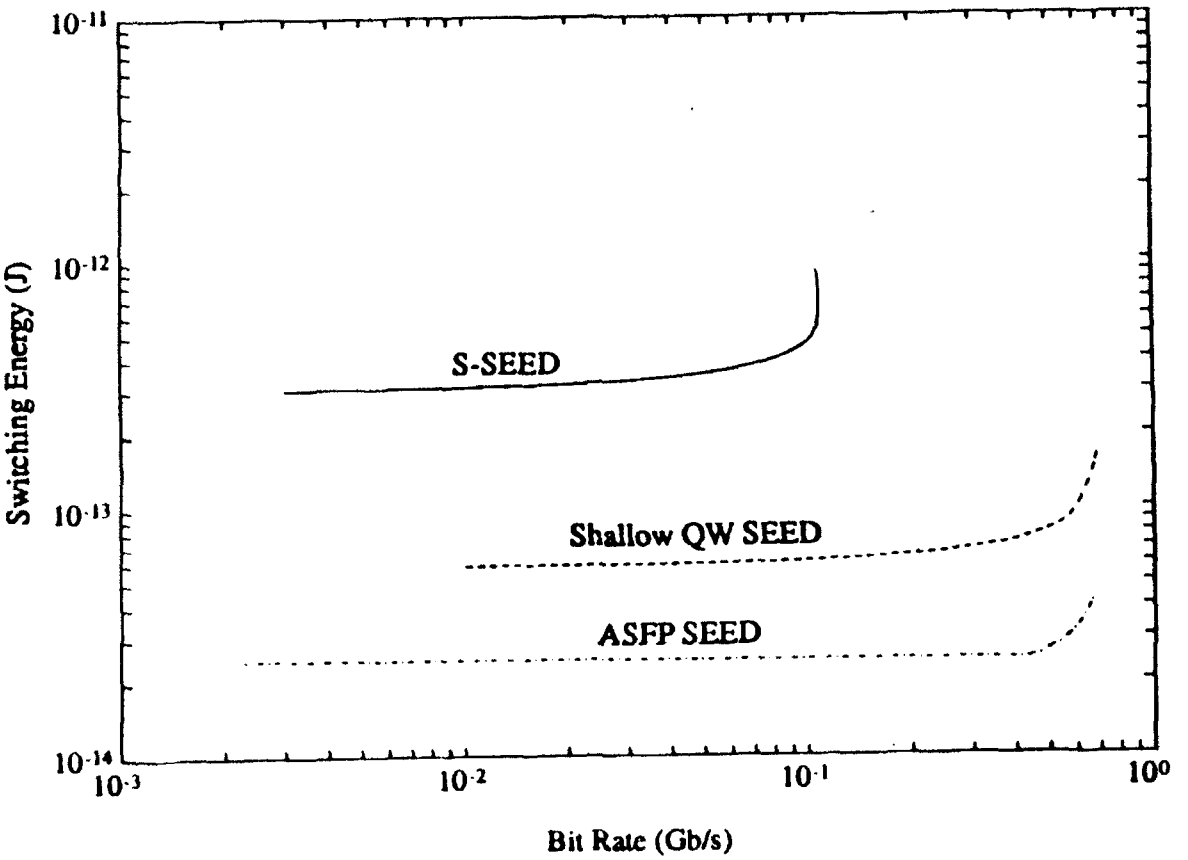

Contrast Ratio
4
3.5
3
2.5
2
1.5
1
0.5
0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
S-SEED
Shallow QW SEED
P_{clk} (mW)

Fig. 8


Switching Energy (J)
10-11
10-12
10-13
10-14
S-SEED
Shallow QW SEED
ASFP SEED
10-3
10-2
10-1
100
Bit Rate (Gb/s)

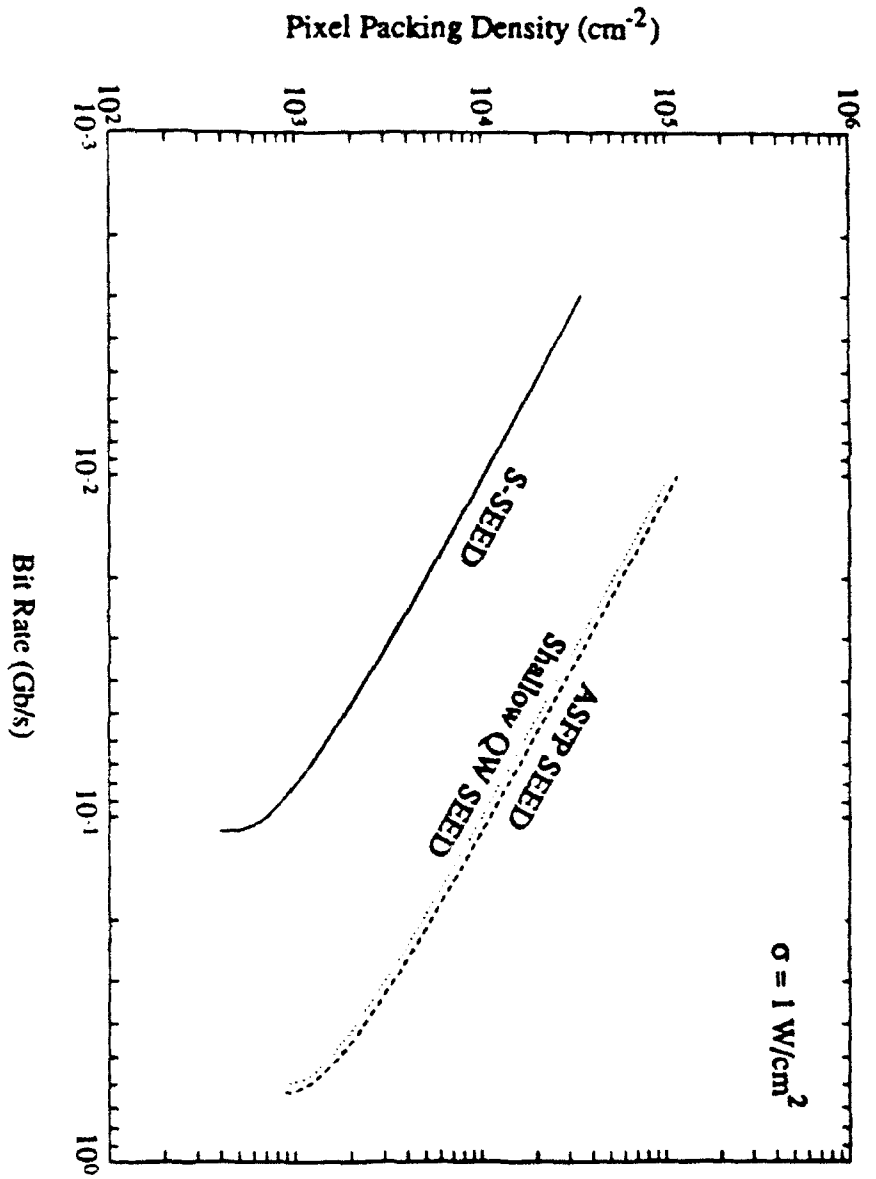
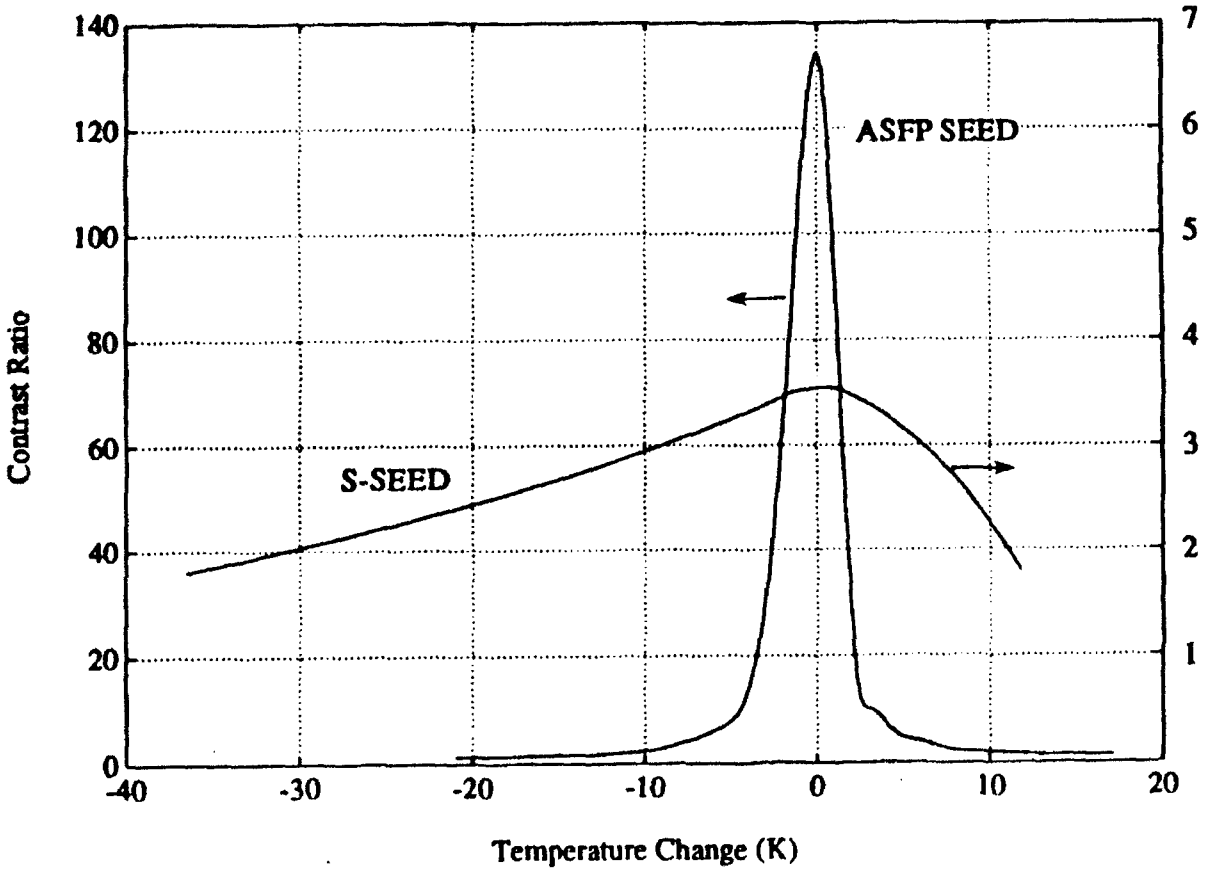
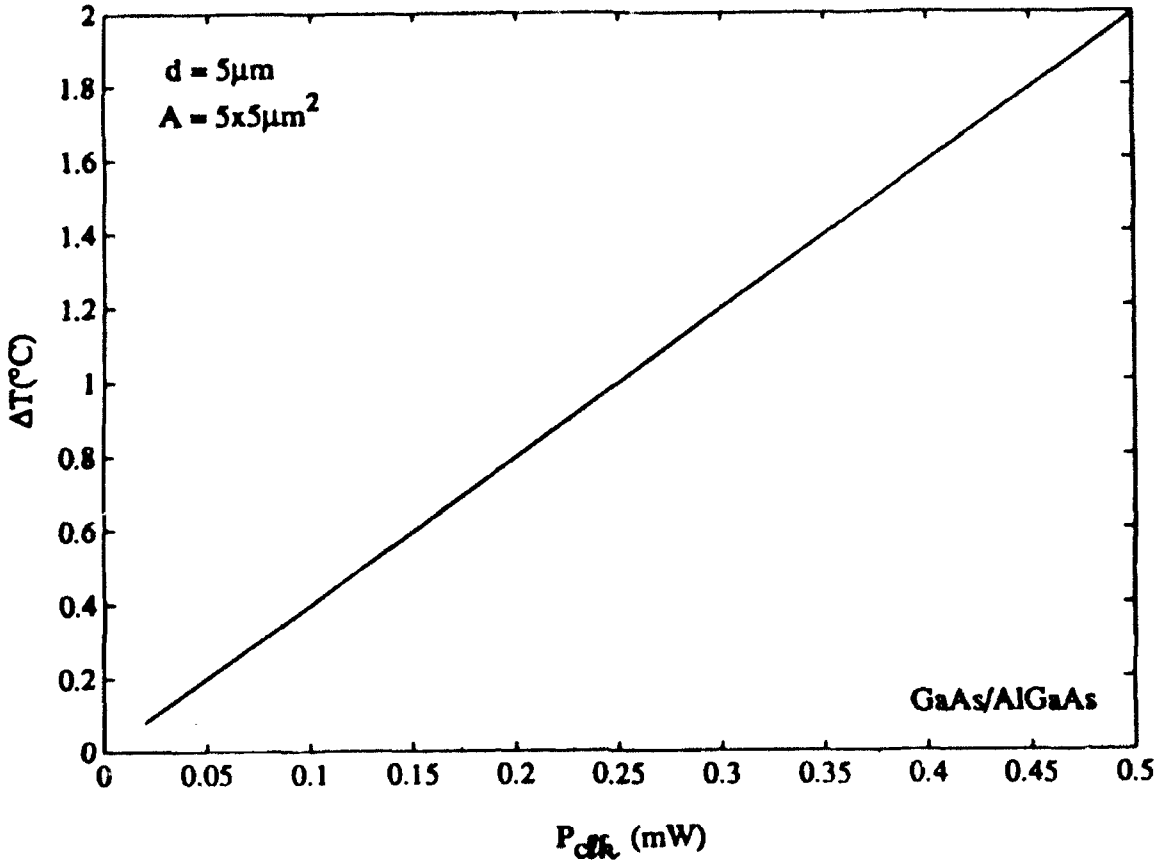

Pixel Packing Density (cm^{-2})
10^{2}
10^{3}
10^{4}
10^{5}
10^{6}
Bit Rate (Gb/s)
10^{-3}
10^{-2}
10^{-1}
10^{0}
S-SEED
Shallow QW SEED
ASFP SEED
σ = 1 W/cm^2

Fig. 9


140
120
100
80
60
40
20
0
7
6
5
4
3
2
1
-40
-30
-20
-10
0
10
20
Contrast Ratio
Temperature Change (K)
ASFP SEED
S-SEED


d = 5μm
A = 5x5μm²
GaAs/AlGaAs
ΔT(°C)
P_dth (mW)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5

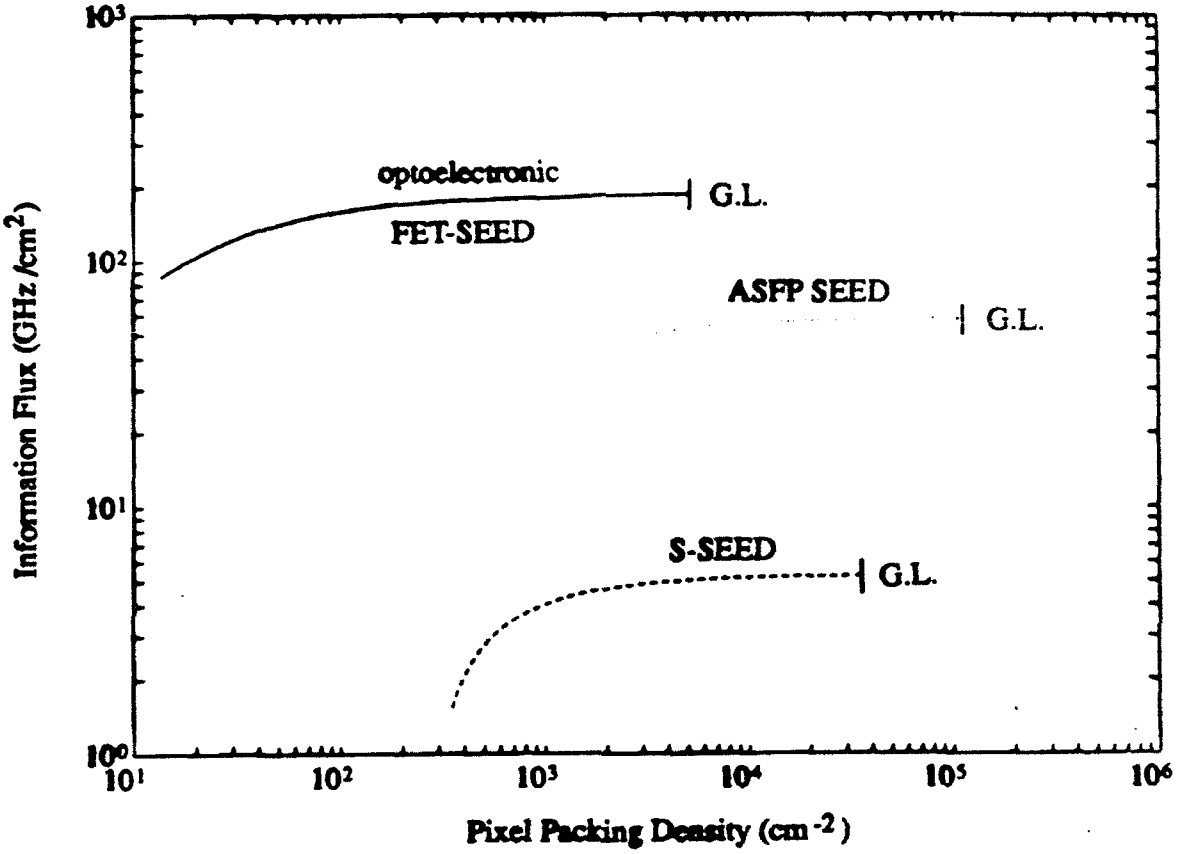

Information Flux (GHz/cm^2)
10^3
10^2
10^1
10^0
optoelectronic
FET-SEED
G.L.
ASFP SEED
G.L.
S-SEED
G.L.
10^1
10^2
10^3
10^4
10^5
10^6
Pixel Packing Density (cm^{-2})

Fig. 12

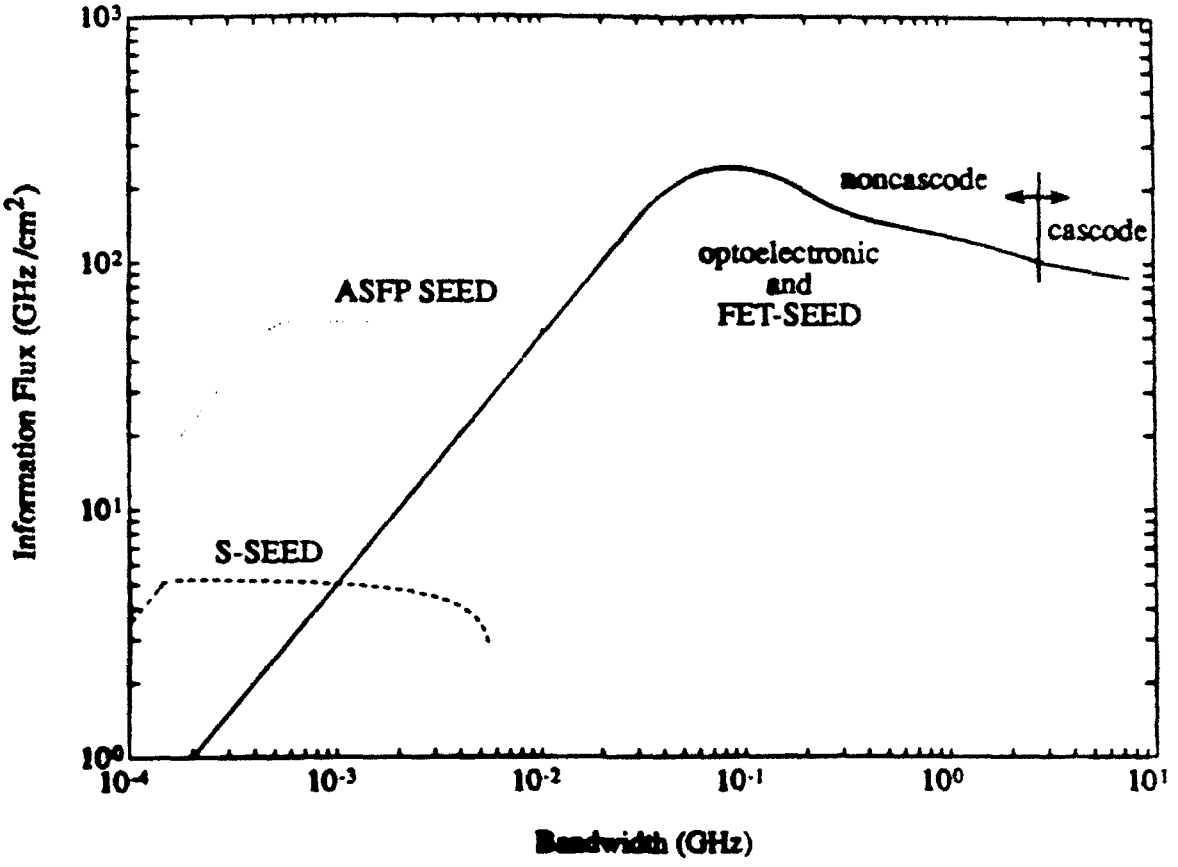

Information Flux (GHz/cm²)
Bandwidth (GHz)
ASFP SEED
S-SEED
optoelectronic
and
FET-SEED
noncascode
cascode

Fig. 13

Switching Noise in Self-Electrooptic Effect Device Logic Gates

Song Yu and S.R. Forrest

Advanced Technology Center for Photonics and Optoelectronic Materials

Department of Electrical Engineering

Princeton University

Princeton, NJ 08544

Abstract

We study the fundamental noise processes of SEED-based logic gates. The switching noise is calculated for symmetric SEEDs (S-SEEDs), asymmetric Fabry-Perot S-SEEDs (ASFP S-SEEDs), and SEEDs combined with transistor driving circuits (FET-SEEDs). The source of noise which determines the minimum power required to switch the SEEDs in a given time increment is quantum noise associated with the photon absorption and subsequent carrier or exciton recombination. The results show that FET-SEED logic gates require the lowest minimum time-average input power as compared with S-SEEDs and ASFP S-SEEDs.

Switching Noise in Self-Electrooptic Effect Device Logic Gates

Song Yu and S.R. Forrest

Advanced Technology Center for Photonics and Optoelectronic Materials

Department of Electrical Engineering

Princeton University

Princeton, NJ 08544

Recent interest in self-electrooptic effect devices (SEEDs) has resulted in their use in several large-scale optoelectronic switching system demonstrations. In such demonstrations, symmetric SEEDs (or S-SEEDs) performed as logic gates in which the output of a S-SEED gate in one stage of a cascaded, 2D network is used to set the state of the S-SEED gate in the following stage [1]. It was apparent from these and other, similar experiments that there is a bandwidth-optical power tradeoff which influences the overall design and implementation of the system. That is, to achieve high bandwidth, it is necessary to use high input power to set the state of the SEEDs. As in the case of optoelectronic gates (with detectors and transistors at the input driving a laser output), the use of a minimum input optical power to achieve a particular bandwidth is desirable since it allows for maximum gate packing density (which is ultimately limited by beam power dissipation), and tolerance for losses of optical signals between stages in the cascade. In considering this bandwidth-power limit, it is useful to determine the fundamental minimum input power required to trigger a S-SEED logic gate. However, to our knowledge, a calculation of this fundamental limit which ultimately determines the performance of S-SEED based architectures, has yet to be presented. It is the purpose of this paper to determine the effect that switching noise has on system performance using these novel device structures.

In a S-SEED logic gate, two series, reverse-biased multiple quantum well (MQW) p-i-n diodes function as both light modulators and photodetectors. Ideally, the switching

process occurs whenever the ratio of the power of the two input beams incident on the series SEEDs (P_{in1}/P_{in2}) becomes large enough such that the photocurrent in one diode significantly exceeds that in the other. Practically , there is a "decision level" determined by the difference of the two input powers which change the state of the S-SEED logic gate. Now, the switching time of a S-SEED is given by [2]:

$$\Delta t = \int_{V_o}^{0} \frac{C_{tot} dV_2}{S(V_o - V_2)P_{in1} - S(V_2)P_{in2}} \tag{1}$$

where V_O is the power supply voltage, V_2 is the voltage across device "2" in the series, C_{tot} is the total S-SEED capacitance, and $S(V)$ is the responsivity [2]. Using Eq. (1) and a supply voltage of V_O=20V, we calculate the changes of the transmission coefficients for the two diodes of the S-SEED during switching at different input power levels. The results are shown in Fig. 1. Note that at the point where the transmission coefficients of the two diodes are equal, the state of the S-SEED is changed. The transmission coefficient corresponding to this point is then defined as the decision level, D. If the time slot, $2\Delta t = 1/B \approx 1/2\Delta f$ (where B is the bit rate and Δf is the bandwidth), is too short for a given input power, then the transmission levels of the two devices will be too close to D such that a switching error occurs. The power levels at the two inputs determine how fast the S-SEED will switch, whereas the ratio of the two input powers (or the contrast ratio in a cascaded system), determines whether the S-SEED will switch within a given time slot. Note that the factor of two in the relationship between Δt and B results since two time slots are required to both set and then to read the S-SEED state. This two-step process is sometimes referred to as "time sequential gain" [1] since the reading power (P_{clk}) can be made larger than the switching power (P_{in}) to make up for losses between cascade stages.

Since the optical power level ranges from microwatts to milliwatts, we can assume that Gaussian noise statistics apply. Hence the probability of a switching error occurring in a time slot, Δt, is given by:

$$p(E) = \frac{e^{-Q^2/2}}{\sqrt{2\pi}Q} \tag{2}$$

where $Q = \frac{D - s_i}{\sigma_i}$. Here, s_i is either $T(V_o)$ or $T(0)$ (i.e. the SEED transmission coefficient at $V = V_o$ or $0V$, respectively), and σ_i is the standard deviation of $T(0)$ or $T(V_o)$. For a given bit error rate (BER) to be achieved by a S-SEED logic gate, a certain value of Q is required. For example, if $p(E) = 10^{-12}$ which is desirable in many applications in optical information processing, then $Q = 7$. This implies that the difference between $T(0)$ and $T(V_o)$ must be $> 14\sigma_i$.

Since the photocurrent of the SEED is due to the absorption of photons, σ_i can be represented by the noise current generated in the device: $\sigma_i^2 = \langle i_q^2 \rangle$, where $\langle i_q^2 \rangle$ is the quantum noise associated with photon absorption and subsequent carrier recombination. Assume that the average number of photons absorbed by the SEED during time slot Δt is N_O, given by:

$$N_o = (P_{in1} + P_{in2}) S(V_o) \Delta t / q = \frac{(CR+1) T(0) S(V_o) P_{clk} L}{2qB}, \tag{3}$$

where $CR = T(V_o)/T(0)$ is the contrast ratio, and L represents the optical losses between stages (which equals the coupling efficiency divided by the logic gate fanout). Since the quantum noise is the standard deviation of the input signal, then $\langle i_q^2 \rangle$ is given by:

$$\langle i_q^2 \rangle = [2q\sqrt{N_o}B]^2 = [4q\sqrt{N_o}\,\Delta f]^2 = 2qB(CR+1)T(0)S(V_o)P_{clk}L, \tag{4}$$

where $\sqrt{N_o}$ is the root mean deviation of N_O. Thus, $\langle i_q^2 \rangle$ is simply equal to the square of the shot noise current in the SEED under illumination. The minimum input power required for setting the logic state of the S-SEED at a given BER is:

$$P_{min} = \left[\frac{CR+1}{CR-1}\right] \frac{Q}{S(V_o)} \langle i_q^2 \rangle^{1/2}. \tag{5}$$

That is, P_{min} depends on the output power of the previous stage times the loss of power between stages ($= P_{clk}T(V)L$). For a typical S-SEED, the CR is between 2 and 4, and the transmission coefficient of the "off" diode is typically $T(0) \cong 0.15$. Figure 2 shows P_{min} vs B for BER = 10^{-12}. The shaded area indicates the bit rate "cutoff region" in which the required BER cannot be achieved. We can see that for low P_{clk}, P_{min} is low while the

cutoff of B (B_{co}) is also low. To increase B_{co}, high P_{clk} is required which will also lead to a proportionate increase in $P_{min} = T(V)P_{clk}L$. Note that since the output of one stage (P_{clk}) is the input which must set the state of P_{clk} in the second stage of a cascaded array configuration, we can define the ratio of P_{clk} to P_{min} as the logic gate "dynamic range". From Fig. 2, we see that for a S-SEED to operate at $100Mb/s$, the input power would be $P_{in} = P_{clk}T(0) = 500\mu W \bullet\ 0.15 = 75\mu W$ and $P_{min} \approx 2\mu W$. Hence , the dynamic range, $P_{in}/P_{min} \approx 15dB$, which is comparable to that of optoelectronic NOR gates operating at $1Gb/s$ [3].

To improve the noise performance of the S-SEED, $T(0)$ should be minimized for a given contrast ratio. The role of contrast ratio is not obvious since it can be increased either by increasing the transmission coefficient of the "on" diode, or by decreasing that of the "off" diode. The ASFP S-SEED has a $T(0)$ that is very small, and the photocurrent is mostly due to $P_{clk}T(V_o)$. Thus we can expect that the ASFP S-SEED has somewhat improved noise performance as compared with conventional S-SEEDs, while the input power of the logical "1" remains high due to the finite $T(V_o)$. S-SEEDs with shallow quantum well structures have comparable noise performance to ASFP S-SEEDs due to the low bias voltage that is needed for their operation (see Fig. 3).

An alternative, "FET-SEED" [4, 5] technology combines transistor-based input and logic circuits to switch a MQW modulator. For the FET-SEED, the noise performance can be analyzed in a manner similar to that used for the optoelectronic NOR gate employing a p-i-n photodiode and a FET based circuit. Therefore, the noise current of the FET-SEED is given by [6]:

$$\langle i_{FS}^2 \rangle = [\frac{4kT}{R}(1+\frac{\Gamma}{g_m R}) + 2qI_g]I_2 B + 4kT\Gamma\frac{(2\pi C_t)^2}{g_m} I_3 B^3, \qquad (6)$$

where R is the bias resistance for the SEED that functions as a photodetector, I_g is the gate leakage current, $\Gamma \approx 1.1$ for GaAs FETs, and C_t is the sum of the SEED, stray, FET gate-source and gate-drain capacitances. Also, g_m is the front-end FET transconductance, kT is the thermal energy, and I_2 and I_3 are integral transfer functions of

the FET-SEED circuit. Since at the inputs of FET-SEED logic gates, the SEED functions as a p-i-n photodiode, we can expect the noise performance of such logic gates to be similar to that of optoelectronic logic gates. Figure 3 compares the minimum time-averaged input power P_{min} of the S-SEED, ASFP S-SEED, and FET-SEED vs B using $P_{clk} = 500\mu W$ for BER = 10^{-12} in addition to the parameters listed in Table 1. We can see that P_{min} for the FET-SEED is lowest among the three different device structures. The cutoff bit rates of the S-SEED and the ASFP SEED following the treatment of Fig. 1 are also shown in the plot.

In summary, for the S-SEED logic gate to operate at high switching speeds, a high reading beam power (P_{clk}) is desirable, which increases P_{min} proportionally according to Fig. 2. As in the case of optoelectronic gates, low input power results in high sensitivity, but only at low bit rates. Device structures incorporating transistors such as the FET-SEED are preferred to improve the noise performance of SEED-based logic gates.

The authors acknowledge the Air Force Office of Scientific Research (Alan Craig) and the National Science Foundation for partial support of this work.

Figure Captions

Figure 1: Switching transient of S-SEED as a function of P_{clk}. When the transmission coefficients of the two SEEDs are equal, the logical state of the S-SEED changes. The intersection is defined as the Decision Level.

Figure 2: Minimum input power (P_{min}) vs bit rate required for the S-SEED to operate at BER = 10^{-12}. The shaded area corresponds to BER>10^{-12}. B_{co} is the cutoff bit rate.

Figure 3: Minimum input power (P_{min}) required for various SEED-based device structures to operate at BER = 10^{-12} with P_{clk} = 500μW. B_{co} is the cutoff bit rate.

References:

1. D.A.B. Miller, Opt. and Quantuim Electron., vol. 22, pp. S61-S68, 1990.

2. A. Lentine, D.A.B. Miller, L.M.F. Chirovsky, and L.A. D'Asaro, IEEE J. Quantum Electron., vol. 27, pp. 2431-2439, 1991.

3. S. Yu and S.R. Forrest, submitted to IEEE J. Lightwave Technology.

4. T.K. Woodward, L.M.F. Chirovsky, A.L. Lentine, L.A. D'Asaro, E.J. Laskowsky, M. Focht, G.Guth, S.S. Pei, F. Ren, G.J. Przybylek, L.E. Leibenguth, M.T. Asom, R.F. Kopf, J.M. Guo, and M.D. Feuer, IEEE Photon Technol. Lett., vol. 4, pp. 614-617, 1992.

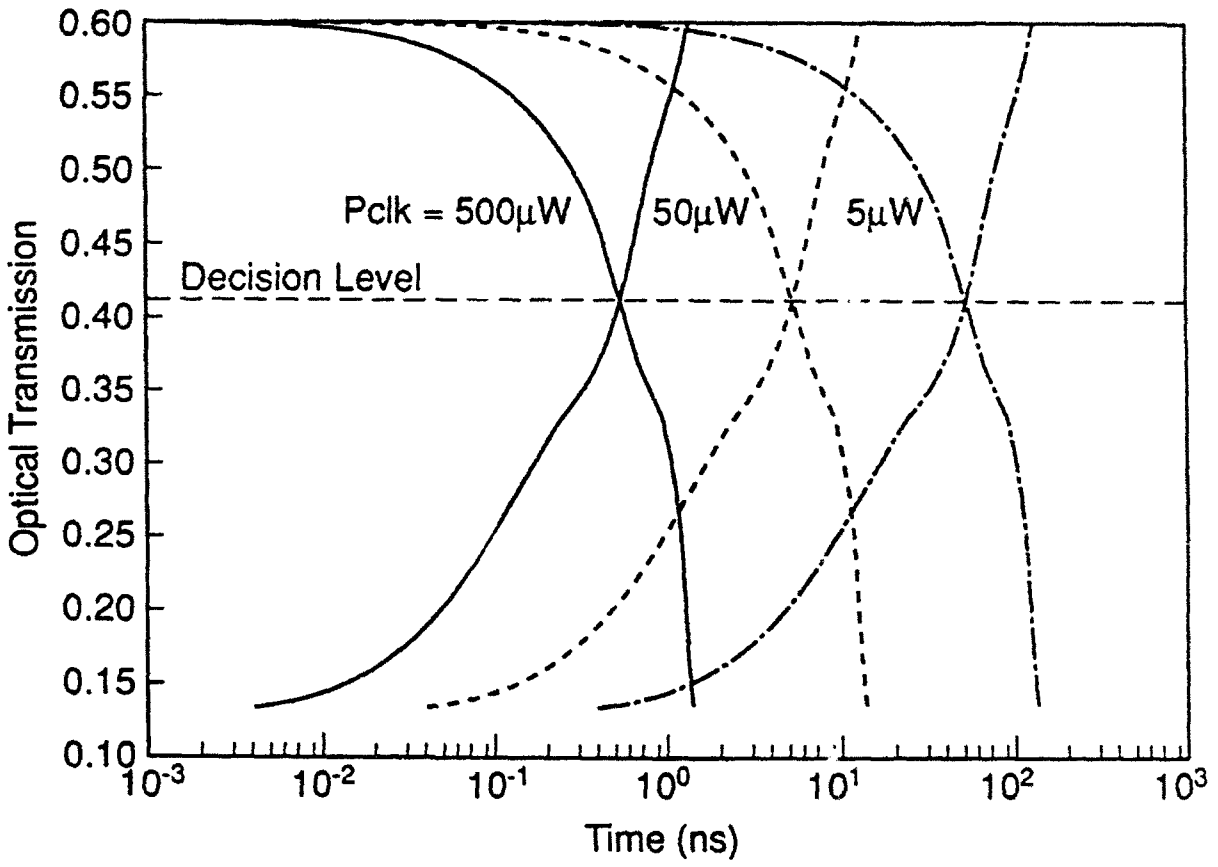
5. T.K. Woodward, A.L. Lentine, L.M.F. Chirovsky, S.S. Pei, J.M. Freund, L.A. D'Asaro, M. Focht, E.J. Laskowsky, G. Guth, and L.E. Smith, IEDM Technical Digest, p.655, 1992.

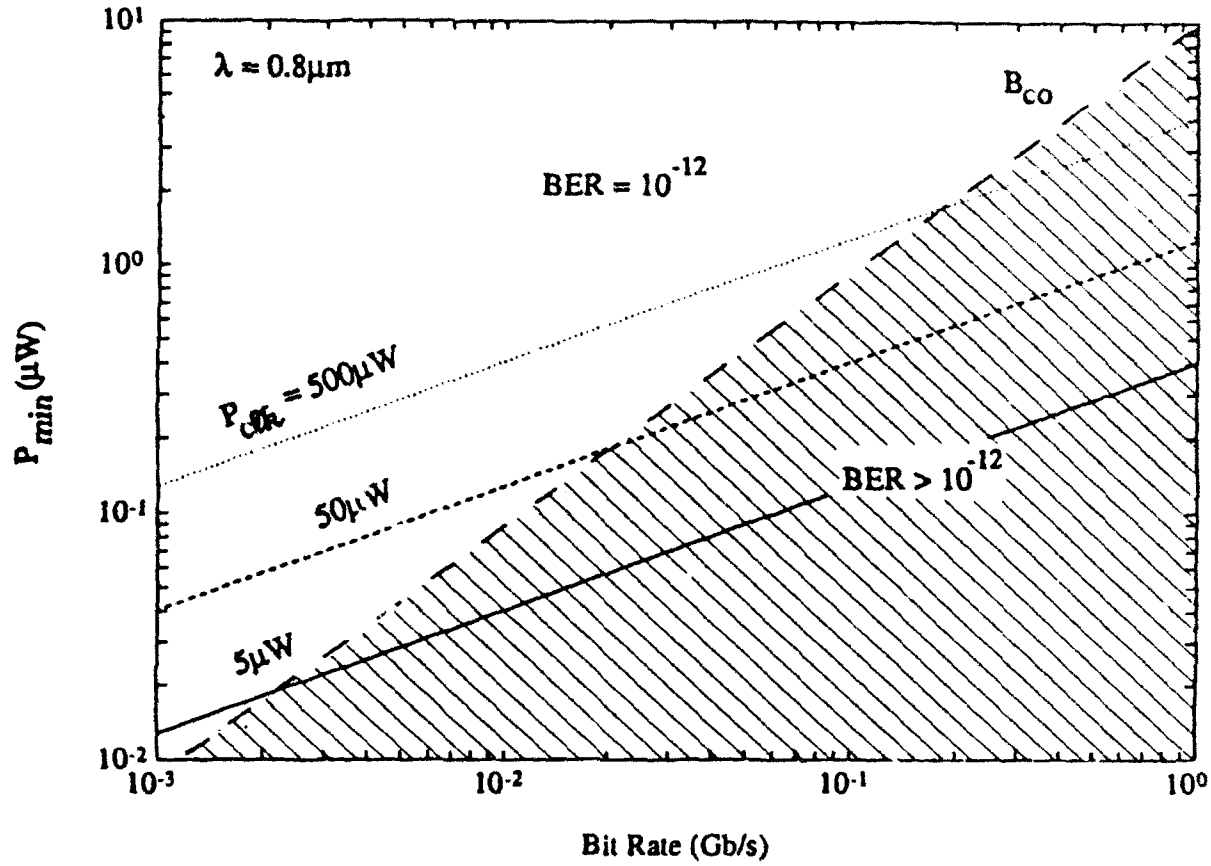
6. R.G. Smith and Personick, "Receiver design for optical communications," Chap. 4, in Semiconductor Devices for Optical Communications, ed. H. Kressel. 1982.

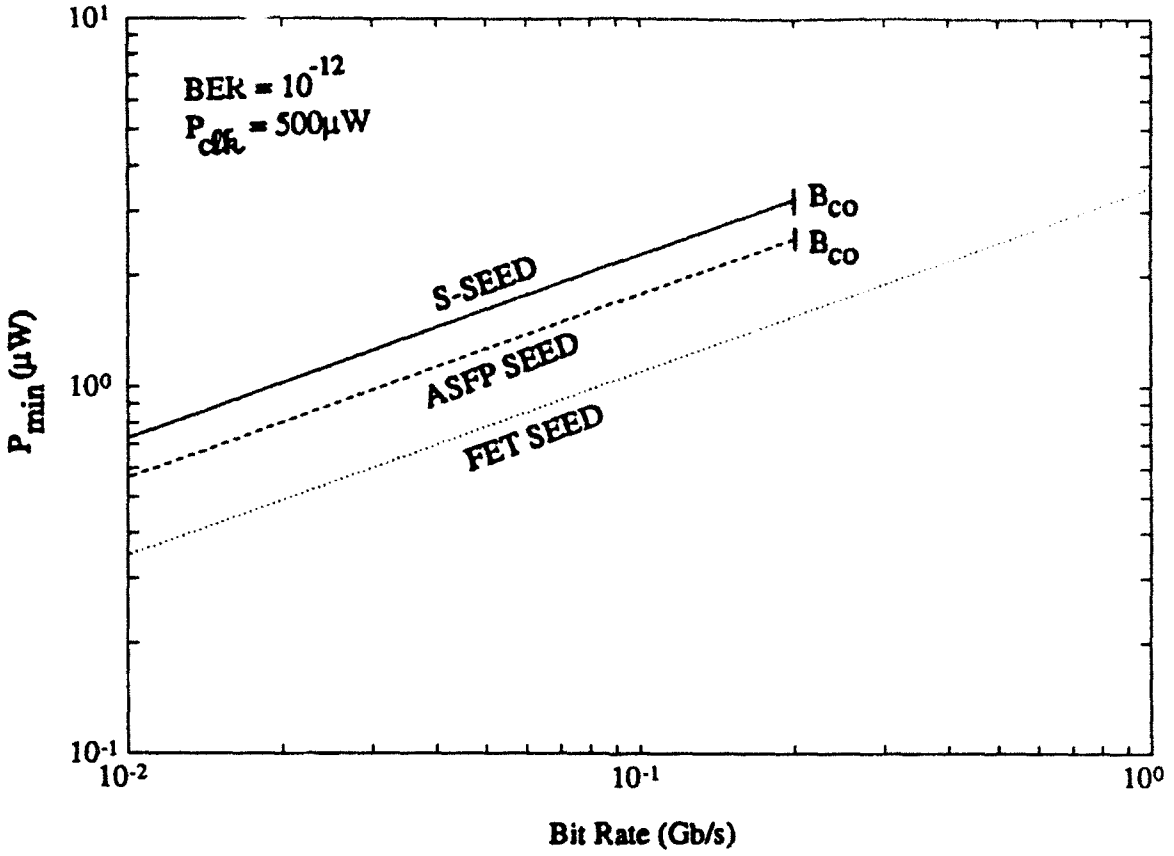
7. R.J. Grindle, J.E. Midwinter, and J.S. Roberts, Electron. Lett., vol. 27, pp. 2327-2329, 1991.

Table 1 Parameters and Performance of SEEDs

	S-SEED	ASFP S-SEED	FET-SEED
Reference	[2]	[7]	[4,5]
SEED Area (μm^2)	5x10	5x5	5x5
V_0 (V)	20	4.2	6
$T(V_0)$ (on)	0.6	0.22	–
T(0) (off)	0.15	0.03	–
CR (@μW)	4(@50)	70	2(@120)
$S(V_0)$ (A/W)	0.31	0.55	–
Quantum Efficiency	–	–	40%
Switching Time (ns)	40	–	2.8
Switching Energy (pJ)	2.5	–	0.1


0.60
0.55
0.50
0.45
0.40
0.35
0.30
0.25
0.20
0.15
0.10
Optical Transmission
Pclk = 500μW
50μW
5μW
Decision Level
10-3
10-2
10-1
100
101
102
103
Time (ns)


10^1
10^0
10^{-1}
10^{-2}
10^{-3}
10^{-2}
10^{-1}
10^0
$\lambda \approx 0.8\mu m$
B_{co}
BER = 10^{-12}
P_{min} (μW)
P_{cw} = 500μW
50μW
5μW
BER > 10^{-12}
Bit Rate (Gb/s)


BER = 10^{-12}
P_{clk} = 500μW
S-SEED
ASFP SEED
FET SEED
B_{co}
B_{co}
P_{min} (μW)
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-1}
10^{0}
Bit Rate (Gb/s)